CDI64600

64-Channel, 16-Bit Current-to-Digital ADC

FEATURES

- 64-channel, current-to-digital converter
- Integrated 16-bit ADC per channel
- Charge amplifier with full scale ranging from 1.75pC to 87.5pC (positive charge)
- Less than 1.5mW per channel
- LVDS interface for data transfer and sequencing
- I^2C interface for device configuration
- Up to 32 devices can be programmed by sharing the same I^2C slave interface.
- Programmable timing for offset and signal sampling
- System clock from 30MHz to 60MHz.
- Accepts positive or negative input current (selection through external reference voltages).

DESCRIPTION

The CDI64600 is a front-end charge amplifier and ADC conversion integrated circuit optimized to offer the lowest power and cost per channel.
The CDI64600 is composed of 64 channels. Each channel includes a charge amplifier and a 16-bit ADC. This combination results in low power consumption and low noise on the IC device.
The CDI64600 is available in a 9x9mm fpBGA, known good dies (KGD) or complete 8” wafers.

APPLICATIONS

- Security and industrial data acquisition
- Photodiode sensors
- X-ray detection systems
- High channel-count data acquisition systems

FUNCTIONAL BLOCK DIAGRAM

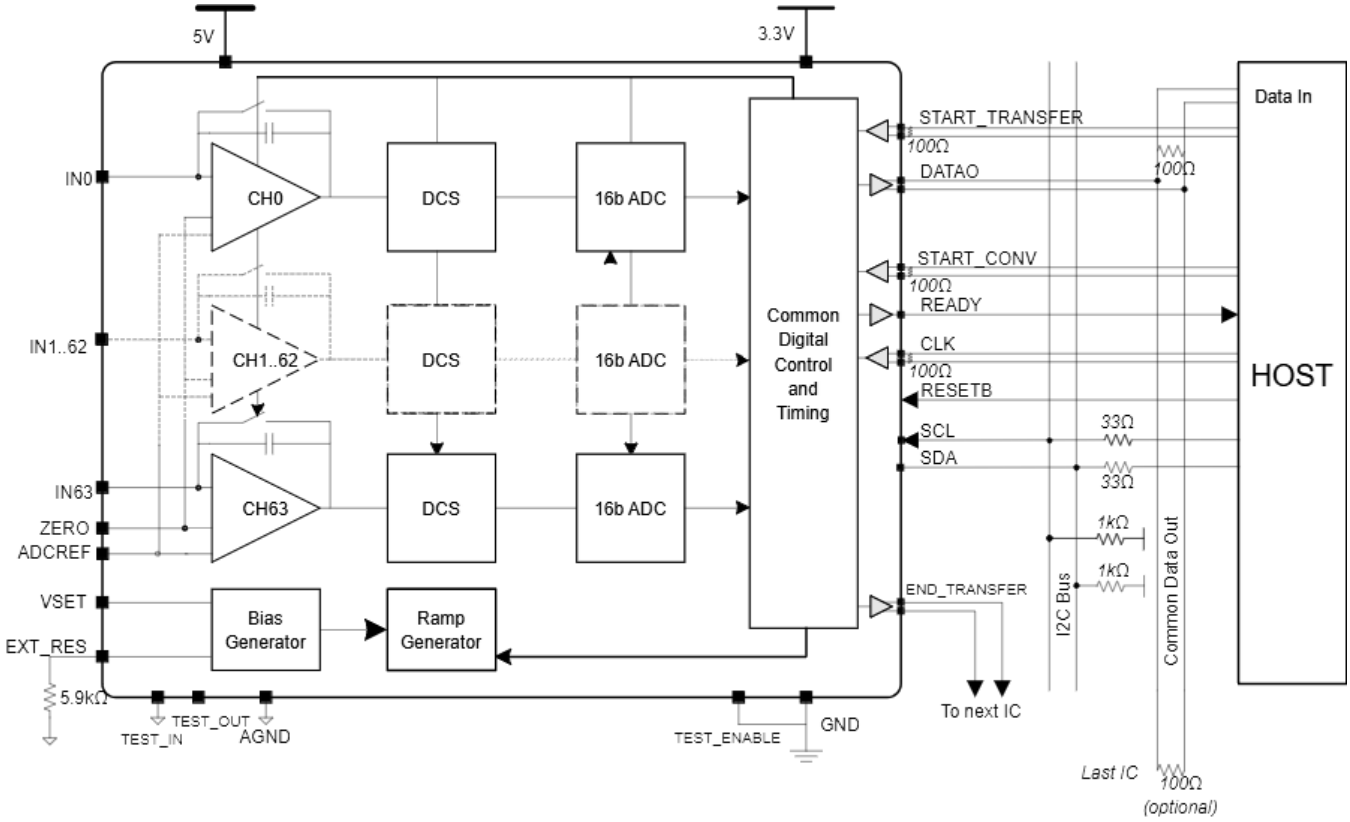

Figure 1: Block diagram

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	*Max*	
Power Supply Voltage (Analog)	VCC		7.0	V
Power Supply Voltage (Digital)	VDD		5.0	V
All input (Analog)		-0.3	VCC+0.3	V
All input (Digital)		-0.3	VDD+0.3	V
Storage Temperature	TSTG	-50	150	°C
Operating Temperature Range	Tamb	-20	80	°C
Lead Temperature (soldering, 10 seconds)	TL		220	°C
ESD HBM Protection on input (Channel input)	Vesdin		1.0	kV
ESD HBM Protection on all pins (except input)	Vesd		2.0	kV

ELECTRICAL CHARACTERISTICS

Parameter description / test conditions	Minimum	Typical	Maximum	Unit
Power Supply Voltages and Current				
Power supply voltage VCC (analog)	4.5	5.0	5.5	V
Power supply voltage VDD (Digital)	3.0	3.3	3.6	V
Operation mode current VCC		10.0		mA
Operation mode current VDD (50MHz) including LVDS drivers.		22.0		mA
Power per channel (50Mhz)		2.0		mW/ch
Charge Amplifier				
Analog output range	0		3.5	V
Feedback capacitor	0.5		25	pF
Full-scale charge (positive or negative input current)	1.75		87.5	pC
Integration dead time per cycle		3	4	us
Digital				
RESETB pulse-width duration	1			us
Delay between the rising edge of RESETB to the first START_CONV	200			clock cycles
ADC				
Conversion clock	30	50	60	MHz
Conversion time @ 50MHz		163.84		us
Resolution (charge amplifier output) (ADCREF=4.00V, VSET=1.00V)			45.78	uV/step
Noise Performance				
Noise with 500fF gain @ 10pF input load		1200		e_{rms}
Noise with 1pF gain @ 10pF input load		1300		e_{rms}
Noise with 2pF gain @ 10pF input load		1700		e_{rms}
Noise with 4pF gain @ 10pF input load		2700		e_{rms}
Communication				
I2C clock rate		400		kHz
I2C input voltage level high VIH	VDD – 0.6			V
I2C input voltage level low VIL			0.6	V
Data clock (system clock)	30	50	60	MHz
LVDS acceptable common mode voltage (Rx)	0.25	1.25	2.25	V
LVDS acceptable differential amplitude (Rx)	100m	350m	-	V
LVDS common mode voltage (Tx)	1.125	1.25	1.375	V
LVDS differential amplitude (Tx)	250m	350m	450m	V

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FUNCTIONALITY

The CDI64600 has 64 channels, and each channel contains a charge amplifier and a 16-bit ADC. The input current (positive or negative) is amplified by a low-noise charge amplifier whose output is captured by a DCS (Double correlated sampling) and then converted to a digital signal in the ADC block. Figure 2 shows the timing of the conversion process.

All the control signals used inside the device are derived from the START_CONV event using a timing table that can be programmed through the I2C interface.

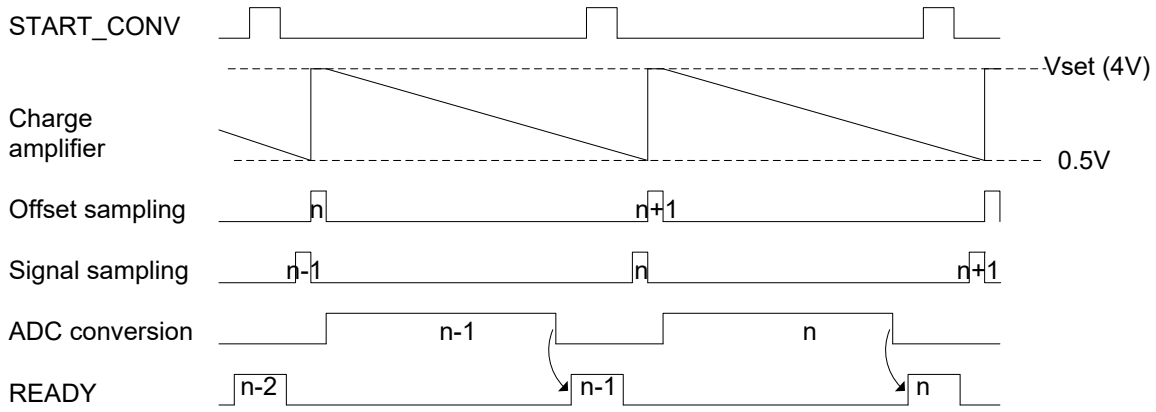

Figure 2: Conversion cycle sequencing

CHARGE AMPLIFIER

The charge amplifier has separate user programmable gains (0.5pF, 1pF, 1.5pF, 2pF, 2.5pF, 3pF, 3.5pF, 4pF) for even and odd groups of 32 channels each. A maximum total programmable gain of 25pF can be achieved by using the additional common bank gains of 6pF and 15pF. The input of the charge amplifier can be operated from 0V to 3.5V. At the end of each conversion cycle, it will be reset to the VSET level (VSET is an externally provided reference voltage). Therefore, the output range of the amplifier will be 3.5V. Then the maximum amount of charge the device can handle is 87.5pC. The charge amplifier can accept positive and negative currents from an external sensor. In the negative current mode, the current flows from the input pin into the charge amplifier. In the positive current mode, the current flows out of the charge amplifier to the input pin. The input current mode is set by the voltage reference VSET and ADCREF, as defined in the Table 1.

Table 1: Voltage reference configuration

Input current mode	VSET	ADCREF
Negative current mode	4.0V	0.5V
Positive current mode	1.0V	4.0V

DOUBLE CORRELATED SAMPLING

After the amplifier is reset, the DCS circuit will sample the offset voltage of the charge amplifier. This operation will last about 2us; any input charge during this period will be lost due to the nature of the DCS circuit. At the highest gain (0.5pF and 1pF), the device will require more settling time, which will increase the offset sampling time (integration dead time per cycle). At the end of the conversion cycle, the DCS captures the output of the charge amplifier and starts the ADC conversion cycle.

ADC

The ADC is a single-slope type where the input voltage is compared with a ramp. A counter is running in parallel with the ramp with a resolution of 2.5ns or 16-bit resolution for a conversion time of 163.84us at a 50 MHz system clock. The device can operate at a system clock frequency ranging from 30 to 60 MHz. The ADC range is defined by the voltage difference between the external VSET and ADCREF.

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OPERATION SEQUENCING

The operation of the CDI64600 is very simple. The frame starts with the host device sending a pulse START_CONV signal. The CDI64600 will sample the output voltage of the charge amplifier and then start the analog-to-digital conversion. At the end of the ADC cycle, the ADC data are collected into a frame buffer. When all channel data is stored in the buffer, the device will activate the READY signal, signalling to the host that it can start to transfer the data out by asserting the signal "START_TRANSFER". As soon as "READY" rises, the device is ready to start a new frame.

For a multi-ASIC configuration, the readout process is done through a daisy chain. The Host sends a START_TRANSFER command to the 1st device that sends its data out through the shared LVDS data line DATAO (from data associated with IN0 to IN63). The 100Ω LVDS receiver terminations are not integrated into the chip. Therefore, the 100Ω terminations must be placed near the LVDS receiver signals of the chips. Figure 1 and Figure 7 illustrate the locations of the 100Ω terminations.

After each conversion, and upon receiving the START_TRANSFER command from the host, the 64 16-bit data words are encapsulated into a data packet starting with a synchronization preamble and ending with a CRC. The readout time for one device is 21.8 us at 50MHz, again not including the LVDS settling time, which is estimated to be at least 16 clock cycles plus latch time (managed automatically by the device). During the LVDS settling time, the DATAO will activate, settle to High and hold it until the synchronization preamble. Refer to Figure 4 for the digital timing diagram.

Details about the Readout data format can be found in the "Readout Data Format" section.

In case the START_TRANSFER command is issued while the READY is not active (0), then no data will be sent out the DATAO lines. This is to prevent reading out data before the internal buffer is ready.

When the 1st device completes its data transfer, it sends a pulse through the "END_TRANSFER" line that is connected to the 2nd device's "START_TRANSFER" input. This process is repeated for all devices in the daisy chain until the "END_TRANSFER" of the last device toggles to signal the end of the readout cycle that lasts up to 349 us for 16 devices (50MHz system clock), or 698 us for 32 devices. Only the READY output of the last device in the chain should be used by the Host. Its rising edge signals that the frame data are ready to be read, while the falling edge signals that all devices have sent their frame data. Because of the frame buffer, a new frame can be started as soon as READY rises, allowing for pipeline operation.

Note: For low noise consideration, the readout cycle should start more than 30us after the START_CONV signal.

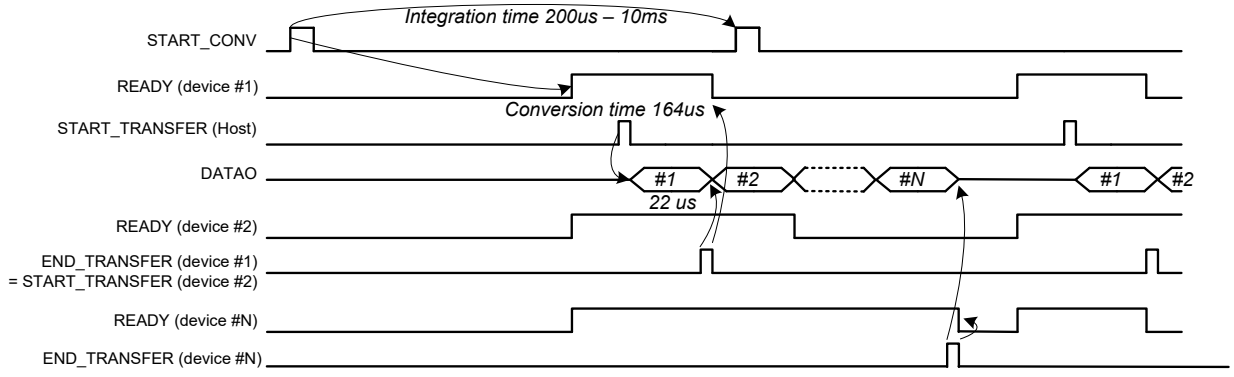

Figure 3: Readout sequencing

The maximum frame rate for 16-bit ADC resolution is 1/200us = 5 kHz for a 50 MHz system clock, providing the data readout is performed in parallel with the acquisition frame. If a higher frame rate is required, the user can reduce the resolution, as shown in the Table 2, which shows the maximum frame rate (kHz) for a given number of ASICs in a daisy chain and resolution (as defined in the timing table):

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Table 2: Maximum frame rate (kHz) table

Resolution (bits)	Number of ASICs in daisy chain					
	1	2	4	8	16	32
14	17.28	17.28	11.49	5.74	2.87	1.44
15	10.12	10.12	11.49	5.74	2.87	1.44
16	5.53	5.53	10.12	5.53	2.87	1.44

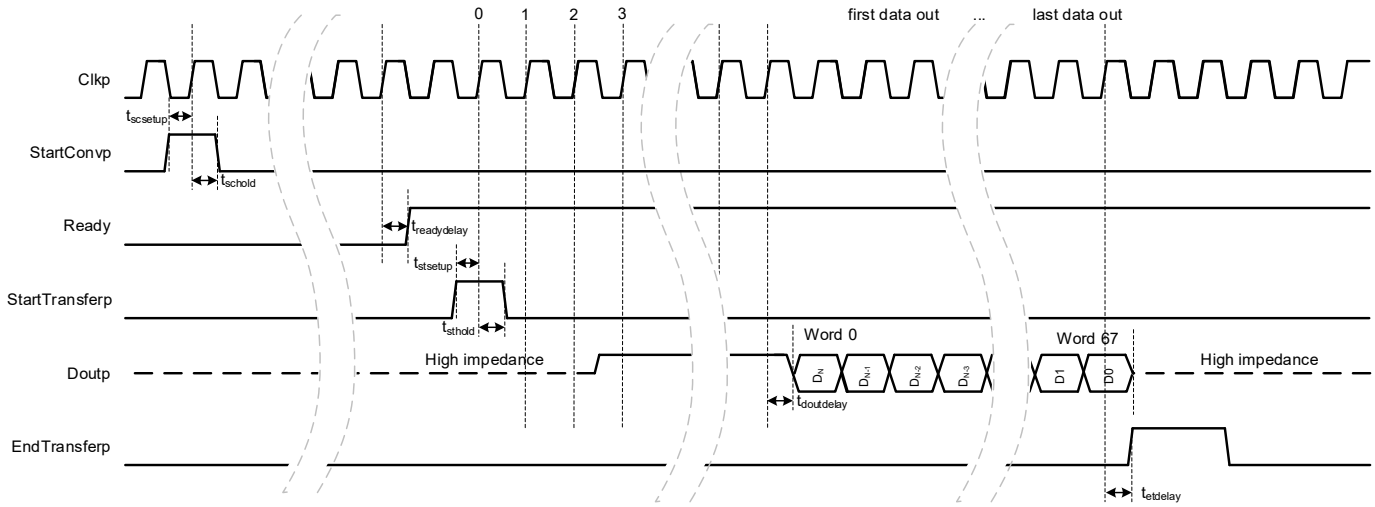

Figure 4: Digital timing diagram (1st daisy chain device) Default readout mode

Table 3: Digital timing specification

Digital switching characteristics	Minimum	Typical	Maximum	Unit
START_CONV setup time ($t_{scsetup}$)	5			ns
START_CONV hold time (t_{schold})	0			ns
CLKP positive edge to READY edge ($t_{readydelay}$)		15	22	ns
START_TRANSFER setup time ($t_{stsetup}$)	5			ns
START_TRANSFER hold time (t_{sthold})	0			ns
CLKP positive edge to Dout edge ($t_{doutdelay}$)	8	11	15	ns
CLKP positive edge to END_TRANSFER edge ($t_{etdelay}$)	8	11	15	ns

USER PROGRAMMABLE FEATURES

The device gain and timing can be programmed through the I2C slave interface. The I2C communication can only be performed when the conversion and readout cycle is completely stopped.

Each device finds its rank inside the daisy chain at start-up by using the END_TRANSFER -> START_TRANSFER daisy chain and uses that information to define its device address, to which it will respond for the I2C communication (the device address will be 0x00 up to 0x1F for the last device of the chain). The devices will start acquiring their respective device address following the reception of a general broadcast I2C frame to the DAACQU register. The general broadcast device address is 0x7F. No data bytes are required. Upon receiving the register address byte, the complete acquisition sequence lasts less than 120 us at a 50 MHz system clock for a daisy chain composed of 32 devices.

Each configuration register is associated with its dedicated address. Multiple registers can be accessed through one I2C frame, provided they have consecutive addresses.

The register map is detailed below.

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Table 4: Register maps

Register ID	Address	Mode	Bits	Meaning	Default value
TIMTABLE	h00-h7F	R/W[1]	7-0	Timing table to control the Front-end and Back-end sequencing. See the table below.	
GAINCTRL	h80	R/W	2-0	Gain selection of the 32 even channels block (inputs IN0, IN2, IN4, ..., IN62). *000b = 0.5pF* *001b = 1pF* *010b = 1.5pF* *011b = 2pF* *100b = 2.5pF* *101b = 3.0pF* *110b = 3.5pF* *111b = 4.0pF*	**h7**
			5-3	Gain selection of the 32 odd channels block (inputs IN1, IN3, IN5..IN63). *000b = 0.5pF* *001b = 1pF* *010b = 1.5pF* *011b = 2pF* *100b = 2.5pF* *101b = 3.0pF* *110b = 3.5pF* *111b = 4.0pF*	**h7**
			6	Add 6pF to feedback capacitor (both bank)	**0**
			7	Add 15pF to feedback capacitor (both bank)	**0**
DIGCTRL	h81	R/W	1-0	Backend test mode control 00 = No test mode enabled 01 = ADC backend test mode[4] 1X = Digital readout logic test mode[5]	**h0**
			2	Reserved	
			3	Phase Generator control (ADC fine step). *0 = phase generator keeps running between frames.* *1 = phase generator stopped between frames.*	**h0**
			4	Abort any current frame, if any. This bit is self-cleared when it is done[6]	**h0**
			5	DCS (Double correlated sampling) *0 = enable* *1 = disable*	**h0**
			6	Ramp gen acquire speed 0 = Normal 1 = Fast	**h0**
			7	0 = Regular data out LVDS drive (3mA)[2] 1 = Double data out LVDS drive (6mA)	**h0**
STATUS	h82	R	0	Busy	**NA**
			1	Phase generator lock[3]	
			2	Timing table checksum validity[7] 1 means valid 0 means invalid	
			3	Signal polarity 1 means that device is configured (through external reference voltages) to process positive input signal, 0 for negative input signal.	
			7-4	Version: Expressed as XXYY where XX is the main version index (value 1 means A), and YY is the minor revision index (value 1 means 01)	

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Register ID	Address	Mode	Bits	Meaning	Default value
TESTCTRL	h83	R/W	0	Input test enable	**h0**
			1	Output test enable	**h0**
			7-2	Channel select (0-63)	**h0**
DAACQU	**hFF**	**-**	**-**	**Start device address acquisition**	**-**

[1]: Access to the TIMTABLE memory space (either for Read or Write) is only allowed if it is not currently used to process a frame (the bit 0 of the STATUS register can be used to monitor that condition). Due to the asynchronous nature of the I^2C access compared to the system clock, any access while busy is asserted can corrupt the TIMTABLE space and yield unpredictable results. If the conversion process hangs up because of an access conflict, the current frame can be aborted using bit 4 of the DIGCTRL register.

[2]: This setting defines the maximum number of devices connected as a daisy chain, depending on system parasitics due to trace and connectors along the LVDS line, as well as termination resistor position (multiple vs single termination).

[3]: If the phase generator status register bit reads 0 consistently, it means that the clock management is not locked. A reset or power cycle is required to reinitialize the clock management. If the phase generator bit reads consistently or intermittently 1, the clock management and chip are functional.

[4]: In this test mode, a token is injected at the input of the digital ADC channel, replacing the comparator outputs. The token travels from one channel to the next every system clock edge, yielding increasing ADC data across the 64 channels. The token travels from the center of the devices toward the edge, so test data decreases from channel 0 to 31, and then increases from channel 32 to 63.

[5]: In this test mode, a digital ADC channel's data are replaced with a pseudo-random test pattern generated by a 16-bit linear-feedback shift register (LFSR) (polynomial $x^{16} + x^{12} + x^5 + 1$) that is reset to the beginning of the sequence (0x0001) every time the register DIGCTRL is accessed in writing. The LFSR advances by one position every time 16-bit ADC data is saved into the double line buffer. Since 2 data words are written at the same time (one for channels 0-31, and the other for channels 32-63) consecutive LFSR codes will be written in non-consecutive channel data locations.

[6]: This command is provided to handle any locked acquisition sequence, related to the bad sequencing inside the timing table (that can happen even if the checksum is Ok). Once the acquisition process is aborted, the internal status of the acquisition sequencer, analog dynamic configuration and data buffer are in an unknown state. At least 2 dummy acquisitions with a proper timing table should be completed before resuming normal operation. The same comment applies In case of a bad timing table checksum.

[7]: That bit is volatile and will be updated at the beginning of each acquisition cycle.

The timing table feature allows the user to customize the sequencing of all the device's internal operations. At power-up, the device reads the default timing table of the IC (ROM-based). This ensures that the device is configured to operate right away. The customer is free to overwrite this table to fit its own needs, and Comport Data will help in writing the timing table contents optimized for specific needs. The default timing table is shown in Table 5 with a conversion time of 200us using a 50MHz system clock. The values written in the table cells show the default start-up state after reset. The minimum delay between the rising edge of RESETB to the first START_CONV is 200 clock cycles. The timing table is read out automatically when the START_CONV input is activated High. From that point, and if the checksum is correct, the table is read line by line. Each line defines what internal control signals to activate and for how long (defined by the 16-bit delay value; minimum 2 clock periods). The table readout stops when the frame completion marker is found inside the column “End Cycle”. If the checksum is not correct, then the acquisition is aborted. The Device will assert its READY output right away, and a monitoring flag inside the readout data stream (in packet mode only) and inside the status register will be set accordingly to indicate that the ADC data are invalid, and the readout data for all channels will be all 1s.

For both test modes, standard ADC sequencing is used, so the checksum inside the timing table must be valid. If not, then the test data will be invalid and read as 0x3FFF, regardless of the readout data mode.

Note: The details about the timing table given below are provided for information only. We strongly suggest customers request Comport Data’s help in designing a custom timing table.

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Table 5: Timing table

		Sub-address (Note 2)	03h	02h	01h								00h								Acquisition phase
		Bit #	7-0 (MSB)	7-0 (LSB)	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Row start address (Note 2)	Total time (ns)	Time increment (ns) (Note 1)	16b delay		Control signals																
					Endcycle	Ready	NC	NC	PG_en	Conv_en	Comp_bias	FE_bias	Comp_reset2	Swap	Ramp_end	Ramp_reset	Signalsample	Offset_sample	Comp_reset	Amp_reset	
00h	0	40	1		0	0	0	0	1	0	1	1	1	1	0	1	0	0	1	0	Turn on all bias& swap
04h	40	5000	249		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	0	Wait for settling
08h	5040	10000	499		0	0	0	0	1	0	1	1	1	0	0	1	1	0	1	0	Sample signal
0Ch	15040	100	4		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	0	Wait
10h	15140	2000	99		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	1	Reset preamp
14h	17140	100	4		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	0	Wait
18h	17240	200	9		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	1	Reset preamp
1Ch	17440	100	4		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	0	Wait
20h	17540	6000	299		0	0	0	0	1	0	1	1	1	0	0	1	0	1	1	0	Sample offset for next cycle conversion
24h	23540	100	4		0	0	0	0	1	0	1	0	1	0	0	1	0	0	1	0	wait
28h	23640	340	16		0	0	0	0	1	0	1	0	1	0	0	1	0	0	0	0	Release analog comp reset
2Ch	23980	180	8		0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	Release ramp_reset
30h	24160	340	16		0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	Release digital comp reset
34h	24500	163700	8184		0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Run conversion time for 16 bit[3]
38h	188200	200	9		0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	End ramp cycle
3Ch	188400	100	4		0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	Wait
40h	188500	6020	300		0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	Save channel data to buffer (262clk)
44h	194520	5260	262		1	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	End cycle
48h	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
4Ch	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
50h	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
54h	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
58h	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
5Ch	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
60h	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
64h	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
68h	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
6Ch	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
70h	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
74h	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
78h	199780	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
7Ch	199780	0	0		0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	0	Timing table checksum[4]

Note 1: Timing increment = [<16b delay value> + 1] x <system clock period> (if <16b delay value> = 0 it is read as 1)
Note 2: <Individual byte address> = <Sub address> + <Row start address>
Note 3: This parameter can be adjusted depending on the resolution by using the formula
<16b delay> = $2^{<Resolution\ in\ bit>-3}$ -8
i.e., 16-bits: 8184 delay, 15-bits: 4088 delays, 14-bits: 2040 delays
In case of a large signal level, the 16-bit readout data will be read as 0xFFFF regardless of this parameter.
Note 4: The 8 LSBs in the table are an 8-bit checksum. When all the bytes in the timing table are summed, the result should be 0xFF.
Note 5: In case no end marker is found (end_cycle = 1), the processing of the timing table will stop at the line before the last one (the line with the checksum is not valid data).

A typical I^2C frame is detailed in the diagram below (1-byte read access). The device is fully compatible with the I^2C protocol, including multi-byte read and write accesses with or without an address setting sub-frame. When the device address defined by the host is 0x7F, for a general broadcast operation, then every device connected to the I^2C bus (up to 32) should accept the data transfer. Of course, this works only for Write access, and it means that if a device doesn't acknowledge the data transfer, it won't be detected.

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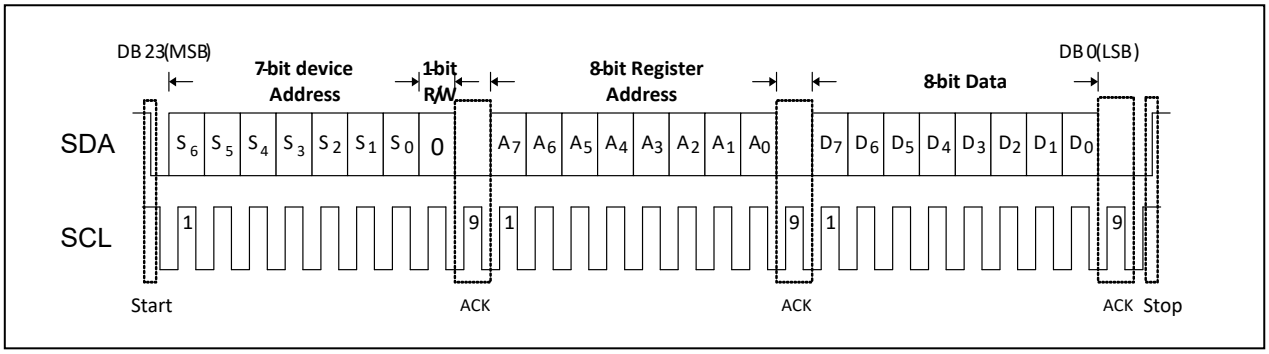

Figure 5: I²C write sequence

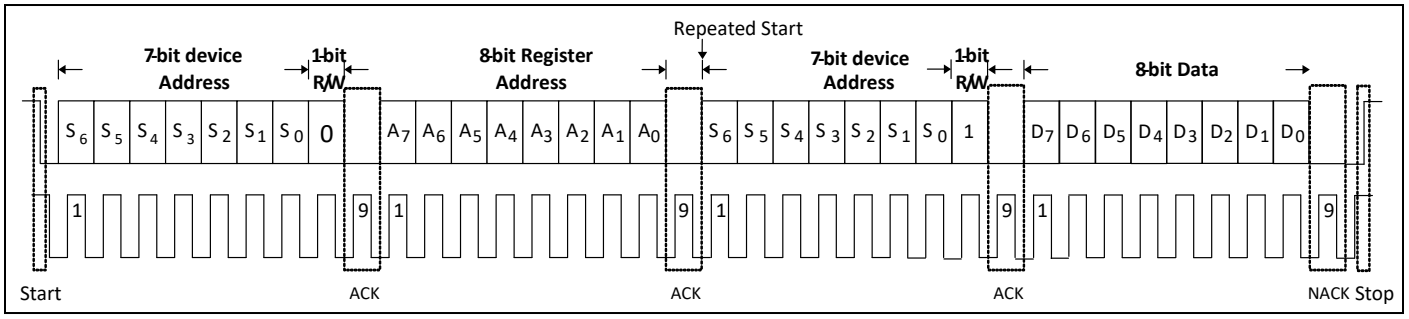

Figure 6: I²C read sequence

READOUT DATA FORMAT

The readout data words are encapsulated into a packet, as follows. The number of bits per data word is kept constant (16 bits) regardless of the resolution defined in the timing table. All words are sent MSB first. The Idle state of the readout line is 1.

Table 6: Readout data format

Word index	Contents	Length (bits)	Comments
0	0xA5 synchronization preamble, MSB first.	8	-
1	Bits 15-0: Packet index.	16	The packet index starts at 0 and is incremented by 1 every conversion cycle. It wraps around the maximum value (0x1FF).
2	Bits 7-0: Configuration checksum Bit 8: Timing table checksum data validity indicator Bits 13-9: 5-bit I2C device address. Bits 15-14: Unused, read as 0x0	16	Sum of all bytes from timing table + registers (I2C address 0x00 – 0x83, except for address 0x82; STATUS register). The host can monitor this checksum to ensure the registers remain valid. When 0, indicates that the ADC data in this packet are not valid, because the checksum of the timing table (I2C address 0x7C) is not correct. - -
3-66	Data words	16	Read as 0x3FFF if the timing table checksum data is invalid (bit 8 of word index 2 is 0).
67	CRC16 of data packet, covering word indexes 1 to 66, MSB first.	16	Based on polynomial $x^{16} + x^{12} + x^5 + 1$, initialized as 0xFFFF before each readout session.

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APPLICATION NOTES

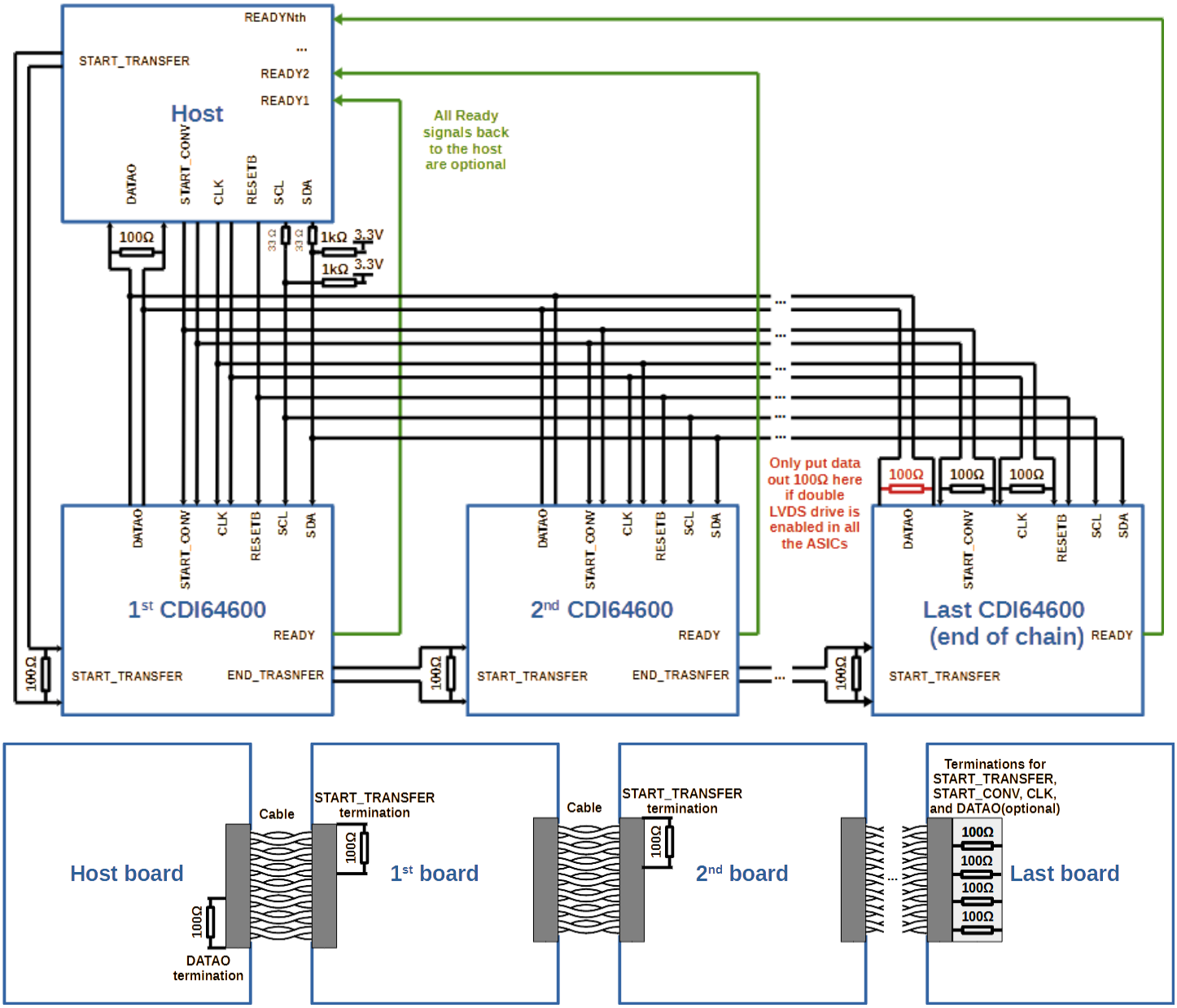

Figure 7: Chip level (top) and Board level (bottom) daisy chain diagrams

The application schematic is illustrated in Figure 1. The daisy chain connections and terminations for multiple chips are shown in Figure 7.

POWER SUPPLY

The Analog section operates on a minimum 5V VCC power supply. It is recommended to set the VCC to 5.2V.

The Digital section VDD operates at 3.3V +/- 5%.

For systems using switching power supplies, we recommend using LDO regulators to ensure a more stable power supply for the chip. Additionally, a combination of multiple decoupling capacitors (10 nF, 100 nF, 1 µF, and 47 µF) should be placed near both the VCC and VDD pins of the CDI64600 to ensure proper filtering and noise suppression, as shown in Figure 8.

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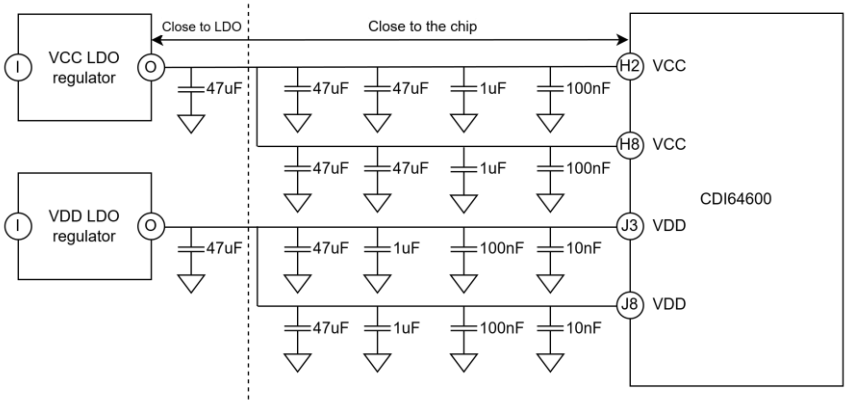

Figure 8: Recommended decoupling capacitors for CDI64600

It is recommended to have a settled clock before powering on the ASIC.

It is recommended to manually reset the ASIC after powering it on to correctly initialize it. The minimum RESETB pulse-width duration is 1us.

ANALOG

VSET pin requires a low impedance, low noise external reference voltage. The output noise of this external reference circuit should be less than 10uV rms. Use a 4.096V reference when operating with the negative current input, and a 0.5V reference for the positive current input.

ADCREF pin controls ADC full-scale range. Use a 0.5V reference for negative current input and a 4.096V reference for positive current input.

The Analog Devices ADR392 precision reference is recommended for generating the 4.096V reference. Its output should be filtered with a 1kΩ/(47uF+100nF) RC network. An OPA350 op-amp, with appropriate output decoupling capacitors, buffers the primary reference. From the buffer reference, a resistor divider can be used to generate a secondary reference. It is also recommended to add 100nF and 10uF decoupling capacitors to the second reference node for additional noise reduction. Figure 9 and Figure 10 show the recommended reference circuits in negative and positive current mode, respectively.

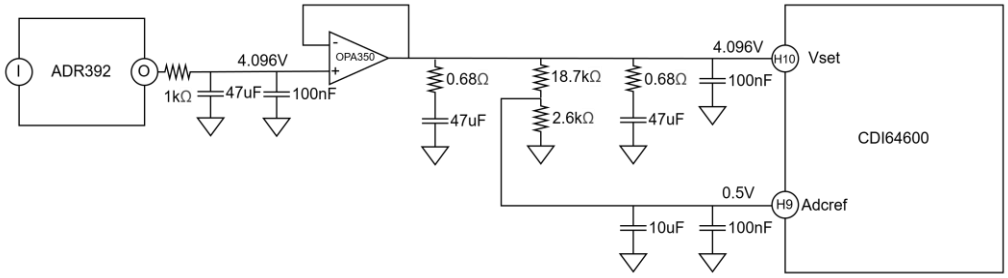

Figure 9: Recommended reference circuit for CDI64600 in negative current mode

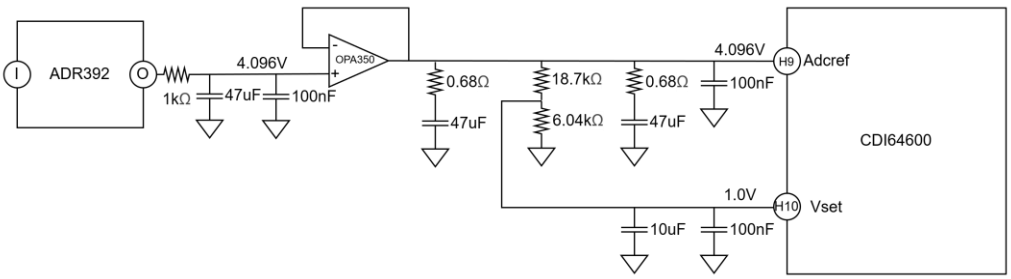

Figure 10: Recommended reference circuit for CDI64600 in positive current mode

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EXT_RES pin is connected to GND through a 5.9kΩ (+/- 1%) default resistor used to provide a constant current bias for all internal circuits, so a low temperature coefficient is required (< 50ppm).

EXT_RES resistor can be changed to improve noise performance depending on the gain settings. For gain ranges <3pF, the EXT_RES resistor can be increased to values as high as 20kΩ. For gain ranges >3.5pF, the EXT_RES resistor can decrease to a value as low as 2kΩ.

TEST_IN should be tied to GND, TEST_OUT should be left floating.

For optimal noise performance, the input channel traces should be shielded and away from digital or noisy signal traces.

ZERO pins are the common positive input of the amplifier. They are connected to the ground of the sensors.

DIGITAL

The recommended operation frequency is 50MHz. Higher frequency (Maximum 60MHz) will reduce conversion time but increase power consumption.

In daisy chain applications, the Host can read out the frame data from up to 32 devices.

The 100Ω termination on the Data Out LVDS network should be located at the end of the daisy chain (farthest from the Host). If the distance between devices is large or includes multiple connectors, bit 7 of RESRCTRL should be set to 1 to increase the drive on the DATAO readout LVDS port.

For systems including many devices or long connection lines between boards, it is strongly suggested to provide a dedicated oscillator per board. Since the data packets on Data Out always start with a synchronization pattern, it is easy for the Host to recover the fine bit synchronization even if the devices are sequenced by asynchronous clocks. A possible way of acquiring synchronization is described below.

The fine synchronization can be achieved inside the Host receiver block by latching the serial data <Line_sync> using 3 copies of the local clock named C1, C2 and C3 and ideally spaced by 1/3rd of a clock period. The result (Q1, Q2 and Q3) will show which clock phase is best suited for data capture later, as shown in the following waveforms.

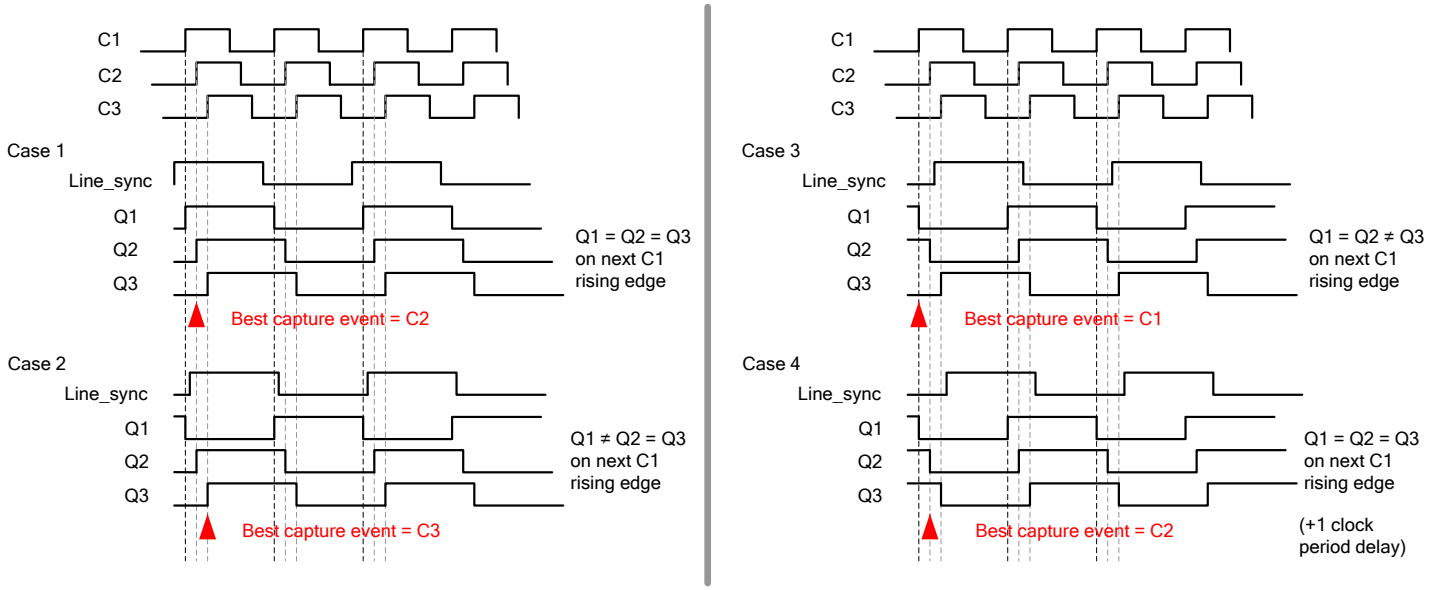

Figure 11: Data Out fine synchronization

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Of course, if <Line_Sync> changes very close to a given clock edge, then multiple cases can be found. However, only the following combinations can coexist.

<Line_sync> close to C1 rising edge: Case 1 / Case2.
<Line_sync> close to C2 rising edge: Case 2 / Case3.
<Line_sync> close to C1 rising edge: Case 3 / Case4.

For all combinations, the capture event associated with each of the 2 possible cases would still be safe. However, a majority vote on 5 consecutive readings can be done to pinpoint the best possible selection (the synchronization pattern is 8-bit long).

The TEST_ENABLE signal should be tied to GND.

For optimal performance, the START_TRANSFER command should be issued 30us after START_CONV is activated.

Set the Ramp Generator Acquire Speed (DIGCTRL register, bit 6) to 1 (Fast) when the ADC resolution is configured to 14-bit or 15-bit, or when aiming for lower noise performance at 16-bit resolution.

For a multiple-ASIC configuration, we strongly suggest inserting 33 to 100Ω series resistors on SDA and SCL, between the Host and the Pullup. The Pullup should be located close to the Host.

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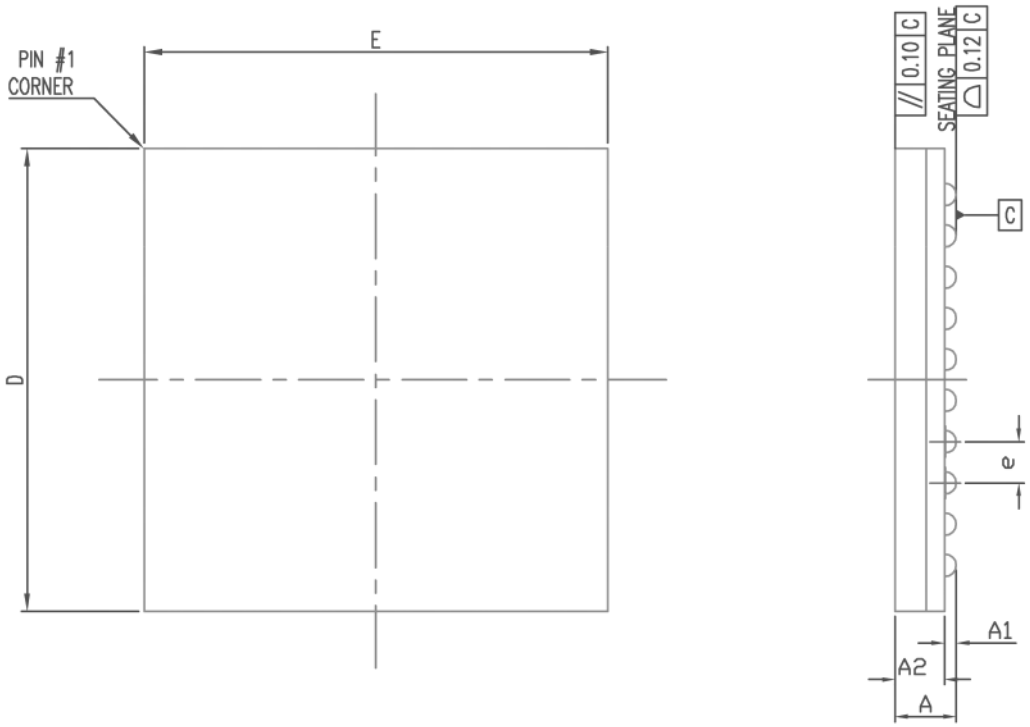
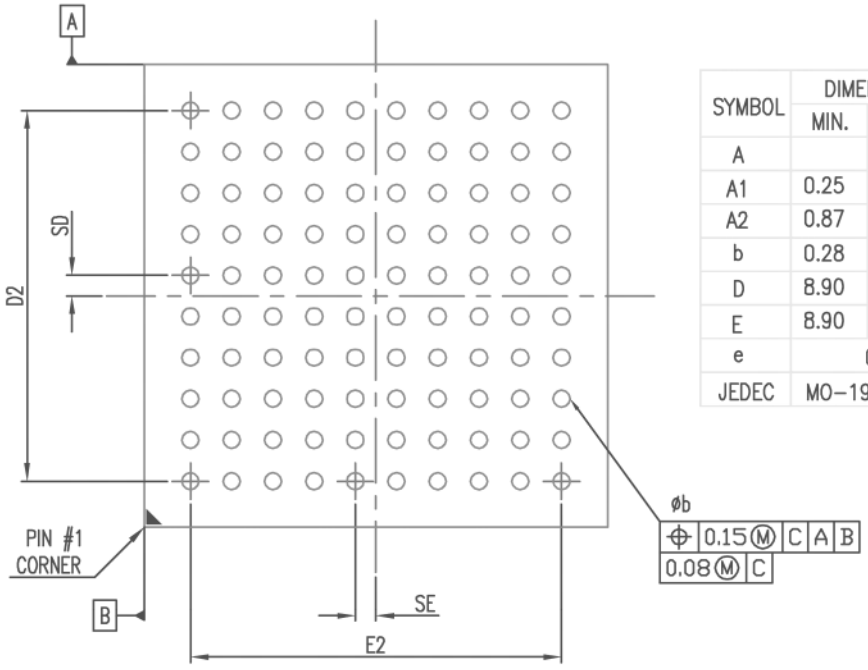
fpBGA PACKAGE DESCRIPTION





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A		1.19	1.33		0.047	0.052
A1	0.25	0.30		0.007	0.009	
A2	0.87	0.96		0.034	0.038	
b	0.28	0.33	0.38	0.011	0.013	0.015
D	8.90	9.00	9.10	0.350	0.354	0.358
E	8.90	9.00	9.10	0.350	0.354	0.358
e	0.80 BSC.			0.031 BSC.		
JEDEC	MO-192,205					

N	SE (mm)	SD (mm)	E2(mm)	D2(mm)	JEDEC(REF)
100	0.40 BSC.	0.40 BSC.	7.20 BSC.	7.20 BSC.	

Ball count: 100; Ball pitch: 0.8 mm; Bond type: Au Ball; Ball size: 460um; Ball material: Lead-free

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fpBGA PIN CONFIGURATION

Top View

	A	B	C	D	E	F	G	H	J	K
1	*ZERO*	*IN13*	*IN12*	*IN10*	*IN6*	*IN5*	*IN0*	*EXT_RES*	*SCL*	*DATAOP*
2	*IN16*	*IN15*	*IN14*	*IN11*	*IN9*	*IN4*	*IN1*	*VCC*	*SDA*	*DATAON*
3	*IN20*	*IN18*	*IN17*	*IN19*	*IN08*	*IN3*	*IN2*	*TEST_OUT*	*VDD*	*END_TRANSFERP*
4	*IN25*	*IN21*	*IN23*	*IN22*	*IN24*	*IN7*	*GND*	*TEST_IN*	*GND*	*END_TRANSFERN*
5	*IN31*	*IN29*	*IN27*	*IN26*	*IN28*	*IN30*	*NC*	*GND*	*GND*	*CLKP*
6	*IN32*	*IN34*	*IN37*	*IN36*	*IN35*	*IN33*	*NC*	*GND*	*TEST_EN*	*CLKN*
7	*IN38*	*IN42*	*IN40*	*IN41*	*IN39*	*IN53*	*GND*	*GND*	*GND*	*START_TRANSFERP*
8	*IN43*	*IN44*	*IN45*	*IN52*	*IN56*	*IN60*	*IN61*	*VCC*	*VDD*	*START_TRANSFERN*
9	*IN46*	*IN48*	*IN47*	*IN51*	*IN55*	*IN59*	*IN62*	*ADCREF*	*RESETB*	*START_CONVP*
10	*ZERO*	*IN49*	*IN50*	*IN54*	*IN57*	*IN58*	*IN63*	*VSET*	*READY*	*START_CONVN*

fpBGA Package
100-Lead, 10x10 array, 9mm x 9mm

PIN LIST

Pin count	Name	Type	Purpose
64	IN0-IN63	Analog Input	Charge input
2	ZERO	Analog Input	Common positive input of the amplifier (Ground)
1	EXT_RES	Analog Input	Bias resistor, low TC (Typical 5.9k to ground)
1	VSET	Analog Input	Low noise reference input (4.0V for negative input current, 1.0V otherwise)
1	ADCREF	Analog Input	ADC Reference (0.5V for negative input current, 4.0V otherwise)
1	TEST_IN	Analog Input	Test input, use this input to inject current into selected channel
1	TEST_OUT	Analog Output	Test output
2	VCC	Power	5V analog power supply
8	GND	Ground	Ground
2	VDD	Power	3.3V digital power supply
2	DATAO(P/N)	LVDS Output	Data out LVDS pair. Drive controlled by bit 7 of register DIGCTRL.
2	START_CONV(P/N)	LVDS Input	Start conversion
2	START_TRANSFER(P/N)	LVDS Input	Start data transfer from ASIC
2	END_TRANSFER(P/N)	LVDS Output	Signals end of data transfer
2	CLK(P/N)	LVDS Input	System clock
1	READY	Output	Data is ready
1	SDA	Open Drain I/O	I2C data line
1	SCL	Input	I2C clock line
1	RESETB	Input	Digital reset pin
1	TEST_ENABLE	Input	Test enable (for production test; should be tied low for normal operation)
2	NC	NC	Not Connected
Total: 100			

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ORDERING GUIDE

Model[1]	Operating Temperature	Package Description	MSL Peak Temp[2]
CDI64600-FBGA[1]	-20°C to 80°C	fpBGA	Level-3-260C-168 HR
CDI64600-KGD	-20°C to 80°C	Bare Die	-
CDI64600-WAFER	-20°C to 80°C	Bare Wafer	-

[1]All models are RoHS compliant part.

[2]MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

REVISION HISTORY

REV	DATE	DESCRIPTION
A01	09/24	Preliminary release
A02	10/24	Update suggested timing table, change ADCREF voltage for positive current mode.
A03	11/24	Corrected CRC16 polynomial, additional information on LVDS settling time, improved description of data validity.
A04	12/24	Ramp gen acquire speed description in the application note, change recommended ADCREF voltage for negative current mode.
B01	12/25	Remove the 100Ω termination inside the chip. Update the default timing table. Add application-recommended figures. Ramp gen acquire speed recommended to be set to 1=Fast for better low noise performance.

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