CDI64500

64-Channel, 18-Bit Current-to-Digital ADC

FEATURES

- 64-channel, current-to-digital converter
- Integrated 18bit ADC per channel
- Charge amplifier with full scale ranging from 1.75pC to 87.5pC (positive charge)
- Less than 1.5mW per channel
- LVDS interface for data transfer and sequencing
- Dedicated I^2C interface for device configuration
- Up to 16 devices can be programmed and read out by sharing the same data lines
- Programmable timing for offset and signal sampling
- System clock from 30MHz to 68MHz

DESCRIPTION

The CDI64500 is a frontend charge amplifier and ADC conversion integrated circuit which is optimized to offer the lowest power and cost per channel.
The CDI64500 is composed of 64 channels. Each channel includes a charge amplifier and an 18-bit ADC. This combination results in low power consumption and low noise on the IC device.
The CDI64500 is available in a 9x9mm fpBGA, known good dies (KGD) or complete 8" wafers.

APPLICATIONS

- Security and industrial data acquisition
- Photodiode sensors
- X-ray detection systems
- High channel-count data acquisition systems

FUNCTIONAL BLOCK DIAGRAM

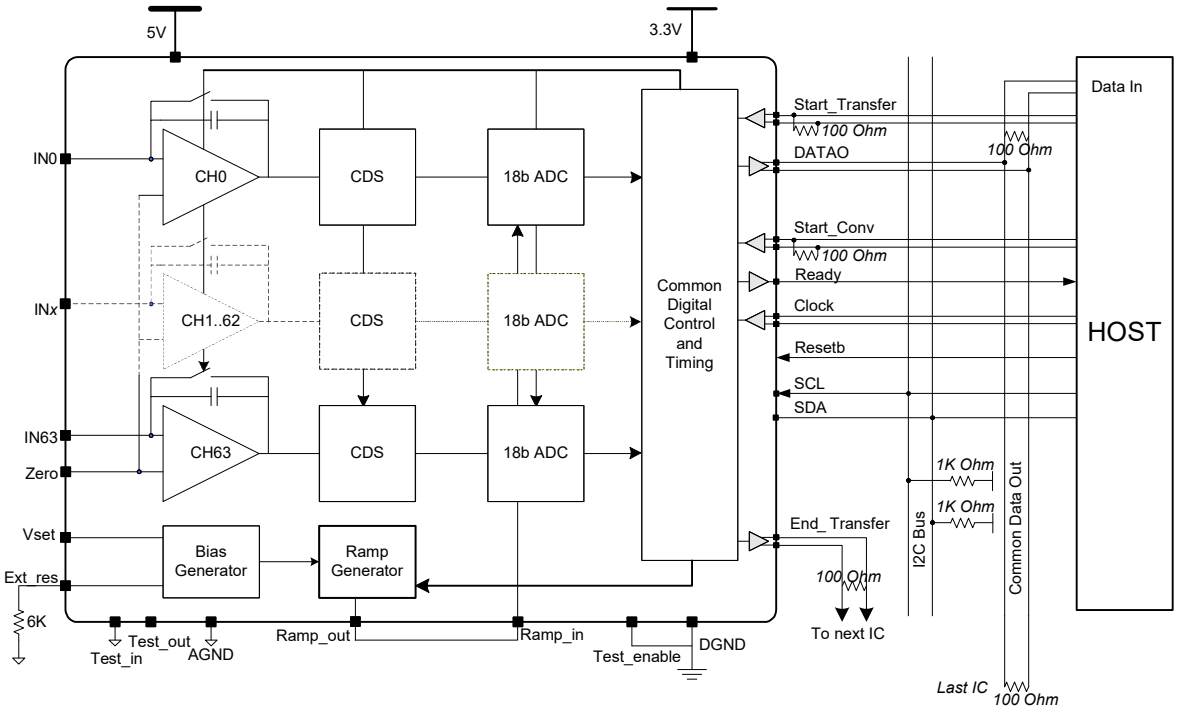

Figure 1.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	*Max*	
Power Supply Voltage (Analog)	VCC		7.0	V
Power Supply Voltage (Digital)	VDD		5.0	V
All input (Analog)		-0.3	VCC+0.3	V
All input (Digital)		-0.3	VDD+0.3	V
Storage Temperature	TSTG	-50	150	°C
Operating Temperature Range	Tamb	-20	80	°C
Lead Temperature (soldering, 10 seconds)	TL		220	°C
ESD HBM Protection on input (Channel input)	Vesdin		1.0	kV
ESD HBM Protection on all pin (except input)	Vesd		2.0	kV

ELECTRICAL CHARACTERISTICS

Parameter description / test conditions	Minimum	Typical	Maximum	Unit
Power supply Voltages and Current				
Power supply voltage VCC (analog)	4.5	5.0	5.5	V
Power supply voltage VDD (Digital)	3.0	3.3	3.6	V
Operation mode current VCC			5	mA
Operation mode current VDD (40MHz) *Including LVDS drivers.*			20	mA
Power per channel		1.25	1.5	mW/ch
Charge Amplifier				
Analog Input range	0		3.5	V
Feedback capacitor (0.5pF, 1pF, 1.5pF, 2pF, 2.5pF, 3pF, 3.5pF, 4pF, 10pF or 25pF)	0.5		25	pF
Full scale charge	1.75		87.5	pC
Integration dead time per cycle		3	4	µs
Digital				
Resetb pulse-width duration	1			µs
Delay between rise edge of Resetb to the first Start_Conv	200			clock cycles
ADC				
Conversion clock	30	40	68	MHz
Conversion time @ 40MHz		430		µs
Resolution (charge amplifier output)			11.4	µV/step
DNL			0.5	LSB
INL			500	ppm*Reading
Offset drift (90 second)		1	2	ppm
Offset drift temperature coefficient		1	2	ppm/°C
Crosstalk Channel to channel			-60	dB
Crosstalk between adjacent conversion cycles			-40	dB
Noise Performance				
Noise with 500fF @ 10pF input load		700		e_{rms}
Noise with 1pF @ 10pF input load		1000		e_{rms}
Noise with 2pF @ 10pF input load		1300		e_{rms}
Noise with 4pF @ 10pF input load		1600		e_{rms}

Communication				
I2C clock rate		400		kHz
I2C input voltage level high VIH	VDD – 0.6			V
I2C input voltage level low VIL			0.6	V
Data clock (system clock)	30	40	68	MHz
LVDS acceptable common mode voltage (Rx)	0.25	1.25	2.25	V
LVDS acceptable differential amplitude (Rx)	100m	350m	-	V
LVDS common mode voltage (Tx)	1.125	1.25	1.375	V
LVDS differential amplitude (Tx)	250m	350m	450m	V

FUNCTIONALITY

The CDI64500 has 64 channels, and each channel contains a charge amplifier and an 18-bit ADC. The input current is amplified by a low noise charge amplifier whose output is captured by a DCS (Double correlated sampling) and then converted to a digital signal in the ADC block. Figure 2 shows the timing of the conversion process.

All the control signals used inside the device are derived from the Start_Conv event using a timing table that can be programmed through the I2C interface.

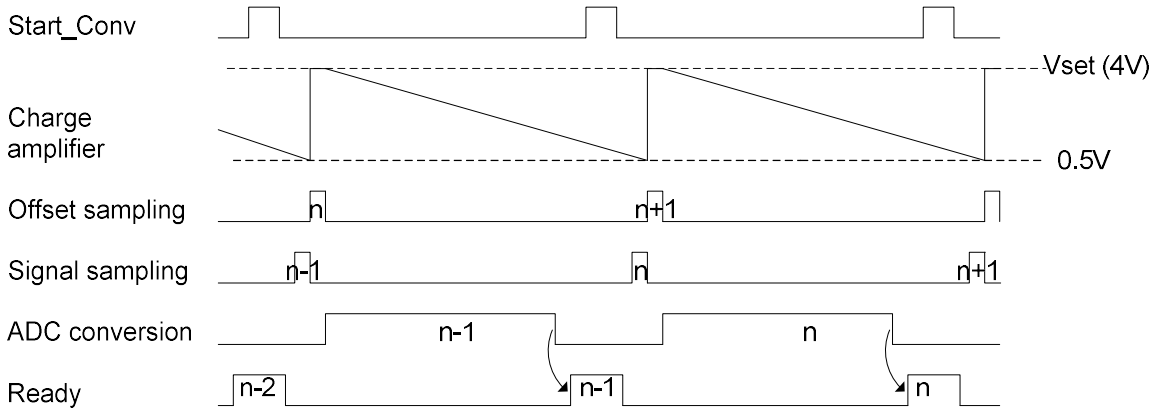


Figure 2: Conversion cycle sequencing

CHARGE AMPLIFIER

The charge amplifier has separate user programmable gains (0.5pF, 1pF, 1.5pF, 2pF, 2.5pF, 3pF, 3.5pF, 4pF) for even and odd groups of 32 channels each. A maximum total programmable gain of 25pF can be achieved by using the additional common bank gains of 6pF and 15pF. The input of the charge amplifier can be operated from 0V to 3.5V. At the end of each conversion cycle, it will be reset to the VSET level (VSET is an external provided reference voltage), therefore the output range of the amplifier will be 3.5V. Then the maximum amount of charge the device can handle is 87.5pC.

DOUBLE CORRELATED SAMPLING

After the amplifier is reset, the DCS circuit will sample the offset voltage of the charge amplifier, this operation will last about 2µs, any input charge during this period will be lost due to the nature of the DCS circuit. At the highest gain (0.5pF and 1pF) the device will require mode time to settling which will increase the offset sampling time (integration dead time per cycle). At the end of the conversion cycle, the DCS captures the output of the charge amplifier and starts the ADC conversion cycle.

ADC

The ADC is a single slope type where the input voltage is compared with a ramp. A counter is running in parallel with the ramp. When the ramp voltage is higher than the input signal, a comparator triggers and captures the value of the counter. A proprietary

phase multiplier circuit produces 16 phases from the input clock (typical 40MHz frequency), which gives us a resolution of 1.56ns or 18b resolution for a conversion time of 409.6 µs. The device can operate at system clock frequency ranging from 30 to 68 MHz.

OPERATION SEQUENCING

The operation of the CDI64500 is very simple. The frame starts with the host device sending a pulse Start_Conv signal. For a multi-ASIC configuration Start_Conv and Clock are fed in parallel to all devices. The CDI64500 will sample the output voltage of the charge amplifier and then starts the analog to digital conversion. At the end of the ADC cycle the ADC data are collected into a frame buffer. When all channel data are stored into the buffer the device will activate the Ready signal, signaling to the host it can start to transfer the data out by asserting the signal "Start_transfer". As soon as "Ready" rises, the device is ready to start a new frame. The maximum frame rate is 1/430 µs= 2.32 KHz for a 40 MHz system clock. If a higher frame rate is required, the user can reduce the resolution as shown in the following table. The resolution is programmed through the I2C interface and will apply on the readout data stream as well.

The following table shows the maximum number of daisy chain ASICs for a selected frame rate (kHz) and resolution (bits):

Resolution (bits) \ Frame rate (kHz)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
14	16	16	12	9	7	5	4	4	3	3	2	2	2	2	1	1	1	1
15	16	16	12	8	6	5	4	3	3	3	2	2	2	1	1	1	1	1
16	16	16	11	8	6	5	4	3	3	2	2	2	2	1	1	1	1	1
17	16	16	10	7	6	4	4	3	3	2	2	2	1	1	1	1	1	1
18	16	15	10	7	5	4	3	3	2	2	2	2	1	1	1	1	1	1

For a multi-device architecture, the readout process is done through daisy chain, i.e. the Host sends a Start_Transfer command to the 1st device that sends its data out through the data line (from data associated with IN0 to IN63). To guarantee enough transitions during the data transfer each 18-bit data word is associated with a start bit, so the readout of a device takes 19 x 64 = 1216 clock cycles, or 30.4 µs at 40 MHz, not including the LVDS settling time that is estimated to be 16 clock cycles plus latch time (managed automatically by the device). The digital switching characteristics and timing diagram are shown in Figure 4.

Note: The multipoint LVDS network associated with Data Out is not driven while no readout is underway. Then a Fail Safe LVDS receiver or a Fail-Safe external termination is required on the receiver side.

When the 1st device completes its data transfer, it asserts an "End_Transfer" line that is connected to the 2nd device Start_Transfer input. This process is repeated for all devices in the daisy chain until the "End_Transfer" of the last device toggles to signal the end of the readout cycle that lasts up to 488 µs for 16 devices. Only the Ready output of the last device in the chain should be used by the Host. Its rising edge signals that the frame data are ready to be read, while the falling edge signals that all devices have sent their frame data. Because of the frame buffer, a new frame can be started as soon as Ready rises, allowing for pipeline operation.

Note: For low noise consideration, the readout cycle should start more than 30µs after Start_Conv signal.

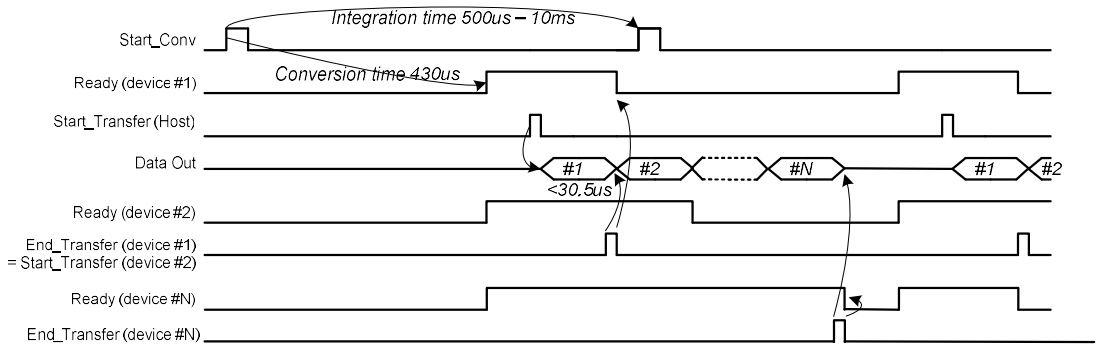


Figure 3: Readout sequencing

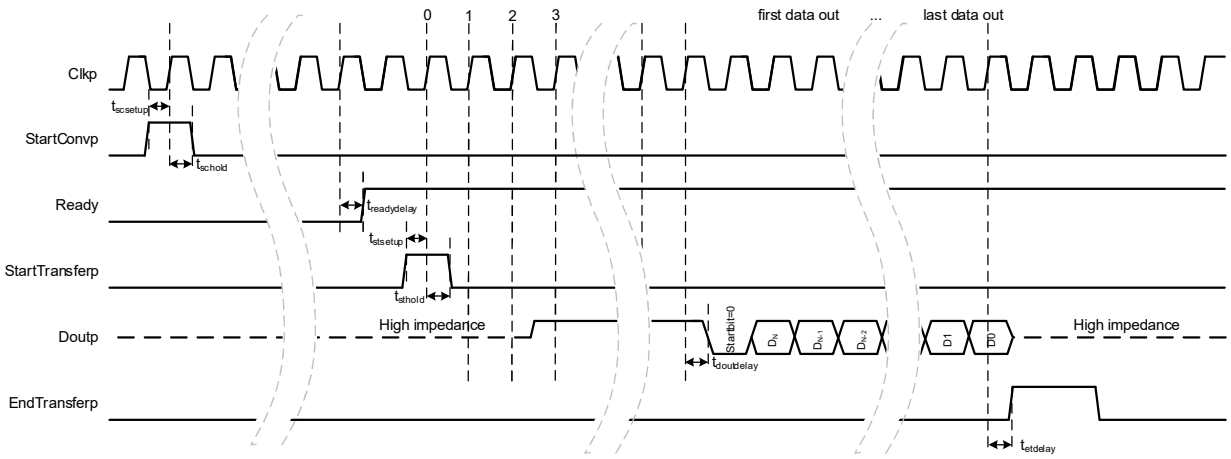


Figure 4: Digital timing diagram

Digital switching characteristics	Minimum	Typical	Maximum	Unit
Start conversion setup time ($t_{scsetup}$)	5			ns
Start conversion hold time (t_{schold})	0			ns
Clkp positive edge to Ready edge ($t_{readydelay}$)		15	22	ns
Start transfer setup time ($t_{stsetup}$)	5			ns
Start transfer hold time (t_{sthold})	0			ns
Clkp positive edge to Dout edge ($t_{doutdelay}$)	8	11	15	ns
Clkp positive edge to End transfer edge ($t_{etdelay}$)	8	11	15	ns

USER PROGRAMMABLE FEATURE

The device gain and timing can be programmed through the I^2C slave interface. The I^2C line must be dedicated and reserved for CDI64500 devices only. The I^2C communication can only be performed when the conversion and readout cycle is completely stopped. Each device finds its rank inside of the daisy chain at start-up by using the End_transfer -> Start_transfer daisy chain and uses that information to define its device address to which it will responds for the I^2C communication (the device address will be 0x00 up to 0x0F for the last device of the chain). The devices will start acquiring their respective device address following the reception of a general broadcast I2C frame associated with the register address byte 0xFF. The general broadcast device address is 0x10. No data bytes are required. Upon receiving the register address byte, the complete acquisition sequence lasts less than 30 µs at 40 MHz system clock for a daisy chain composed by 8 devices. Each register is associated with its dedicated address. Multiple registers can be accessed through one I2C frame providing they have consecutive addresses.

The register map is detailed below.

Table1: Register maps

Register ID	Address	Mode	Bits	Meaning	Default value
TIMTABLE	h00-h7F	R/W[1]	7-0	Timing table to control the Front-end and Back-end sequencing. See the table below.	
GAINCTRL	h80	R/W	2-0	Gain selection of the 32 even channels block (inputs IN0, IN2, IN4 ... IN62). *000b = 0.5pF* *001b = 1pF* *010b = 1.5pF* *011b = 2pF* *100b = 2.5pF* *101b = 3.0pF* *110b = 3.5pF*	h7

Register ID	Address	Mode	Bits	Meaning	Default value
				111b = 4.0pF	
			5-3	Gain selection of the 32 odd channels block (inputs IN1, IN3, IN5..IN63). *000b = 0.5pF* *001b = 1pF* *010b = 1.5pF* *011b = 2pF* *100b = 2.5pF* *101b = 3.0pF* *110b = 3.5pF* *111b = 4.0pF*	h7
			6	Add 6pF to feedback capacitor (both bank)	h0
			7	Add 15pF to feedback capacitor (both bank)	h0
RESCTRL	h81	R/W	2-0	Resolution selection *h0 = 14 bits* *h1 = 15 bits* *h2 = 16 bits* *h3 = 17 bits* *h4 = 18 bits* *All other values reserved.*	h4
			3	Phase Generator control (ADC fine step). *0 = phase generator keeps running between frames.* *1 = phase generator stopped between frames.*	h0
			4	Reserved	h0
			5	DCS (Double correlated sampling) *0 = enable* *1 = disable*	h0
			6	Ramp gen acquire speed 0 = Normal 1 = Fast	h0
			7	0 = Regular data out LVDS drive (3mA)[2] 1 = Double data out LVDS drive (6mA)	h0
STATUS	h82	R	0	Busy[3]	NA
			1	Phase generator lock[4]	
			2	Duty cycle lock[5]	
			7-3	Chip revision number	
TEST	h83	R/W	0	Input test enable	h0
			1	Output test enable	h0
			7-2	Channel select (0-63)	h0
DAACQU	hFF	-	-	Start device address acquisition	-

[1]: Access to the TIMTABLE memory space (either for Read or Write) is only allowed if it is not currently used to process a frame (the bit 0 of the STATUS register can be used to monitor that condition). Due to the asynchronous nature of the I^2C access compared to the system clock, any access while busy is asserted can corrupt the TIMTABLE space and yield unpredictable results.

[2]: This setting defines the maximum number of devices connected as a daisy chain depending on system parasitics due to trace and connectors along the LVDS line, as well as termination resistor position (multiple vs single termination).

[3]: Busy bit indicates when the ASIC is sequencing the timing table for a frame acquisition. In idle state (no start acquisition), the busy bit should be 0. If it is constantly 1 in idle state, the ASIC did not see the end of cycle bit in the timing table and a reset is required to recover.

[4]: Phase generator lock bit switches between 0 and 1 in correct operating condition based on the timing table event.

[5]: Duty cycle lock reads 1 or occasionally 0 in correct operating condition. If duty cycle is stuck at 0, a reset is required to reinitialize the clock management.

The timing table feature allows the user to customize the sequencing of all the device internal operations. The table below represents the default timing table of the IC (ROM-based). The customer is free to overwrite this table to fit its own needs. The default timing table is shown in table 2 below with a conversion time of 430 µs using a 40MHz system clock. The values written in the table cells show the default start-up state after reset. The minimum delay between the rising edge of Resetb to the first Start_Conv is 200 clock cycles. The timing table is read out automatically when the Start_Conv input is activated High. From that point the table is read line by line. Each line defines what internal control signals to activate and for how long (defined by the 16b delay value; minimum 2 clock periods). The table readout stops when the frame completion marker is found inside the column "End Cycle".

Table2: Timing table

		Sub-address (Note 2)	**03h**	**02h**	**01h**							**00h**								
		Bit #	7-0 (MSB)	7-0 (LSB)	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Row start address (Note 2)	Total time (ns)	Time increment (ns) (Note 1)	16b delay		**Control signals**																
					End cycle	Ready	NC	NC	PG_en	Conv_en	Comp_bias	FE_bias	Comp_reset2	Swap	Ramp_end	Ramp_reset	Signal sample	Offset_sample	Comp_reset	Amp_reset	
00h	0	50	1		0	0	0	0	1	0	1	1	1	1	0	1	0	0	1	0	Turn on all bias & swap
04h	50	4825	192		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	0	Wait for Bias ready
08h	4875	10025	400		0	0	0	0	1	0	1	1	1	0	0	1	1	0	1	0	Sample signal for 10µs
0Ch	14900	25	0		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	0	Wait 25ns
10h	14925	475	18		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	1	Reset Charge amplifier for 475ns
14h	15400	50	1		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	0	Wait 50ns
18h	15450	3775	150		0	0	0	0	1	0	1	1	1	0	0	1	0	1	1	0	Sample offset for 3.775µs
1Ch	19225	225	8		0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	0	Wait for 225ns
20h	19450	425	16		0	0	0	0	1	0	1	0	1	0	0	1	0	0	0	0	Release analog comp. reset, turn off charge amplifier bias
24h	19875	825	32		0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	Release ramp generator reset
28h	20700	425	16		0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	Release comparator logic reset
2Ch	21125	409425	16376		0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Run conversion for 18bit (4094 for 16bit)[3]
30h	430550	100	3		0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	End of conversion, end of ramp generator
34h	430650	25	0		0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	Reset ramp generator
38h	430675	50	0		0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	Turn off ramp gen. bias, send Ready signal
3Ch	430725	25	1		1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	End of cycle, wait for Start_conv
40h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
44h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
48h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
4Ch	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
50h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
54h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
58h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
5Ch	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
60h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
64h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
68h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
6Ch	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
70h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
74h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
78h	430750	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
7Ch	430750	0	0		0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	1	

Note 1 : Timing increment = [<16b delay value> + 1] x <system clock period> (if <16b delay value> = 0 it is read as 1)

Note 2 : <Individual byte address> = <Sub address> + <Row start address>
Note 3 : This parameter should be adjusted depending on the resolution configuration (see register RESCTRL defined above) by using the formula

<16b delay> = 2 ^ <Resolution in bits>/16 -8
i.e. 18-bits: 16376 delays, 17-bits: 8184 delays, 16-bits: 4088 delays, 15-bits: 2040 delays, 14-bits: 1016 delays

The meaning of the various control signals is detailed in the table below.

Table3: Control signal meaning

Signal name	***Purpose***
Amp reset	Reset the charge amplifier (<500ns)
Comp reset	Reset the comparator (analog)
Offset sample	Sample the offset value from the Charge amplifier (2µs for gain greater than 1pF, 3µs for gain less than 1.5pF)
Signal sample	Sample the integrated charge from the charge amplifier (8µs)
Ramp reset	Reset the Ramp generator
Ramp end	Mark the end of the ramp generator
Swap	Swap between odd and even offset
Comp reset 2	Reset the comparator logic (digital)
FE bias	Enable the Charge amplifier bias (full bias or 1/8 bias)
Comp bias	Enable the Comparator bias (full bias or ½ bias)
Conv en	Start the conversion cycle
NC	Not used
Ready	Signals the end of the conversion cycle. Triggers the data transfer from the 64 ADCs to a buffer SRAM.
End cycle	Signal the completion of one frame. From that point a new frame can be started through the activation of Start_Conv.

A typical I^{2}C frame is detailed in the diagram below (1-byte read access). The device is fully compatible with the I^{2}C protocol including multi-byte read and write accesses with or without address setting sub-frame. When bit 4 of the device address is High (1), then each device connected to the I^{2}C bus (up to 16) should accept the data transfer. Of course, this works only for write access, and it means that if a device doesn't acknowledge the data transfer it won't be detected. If the bit 4 of the device address is Low (0), then only the device addressed through bits 3-0 should respond.

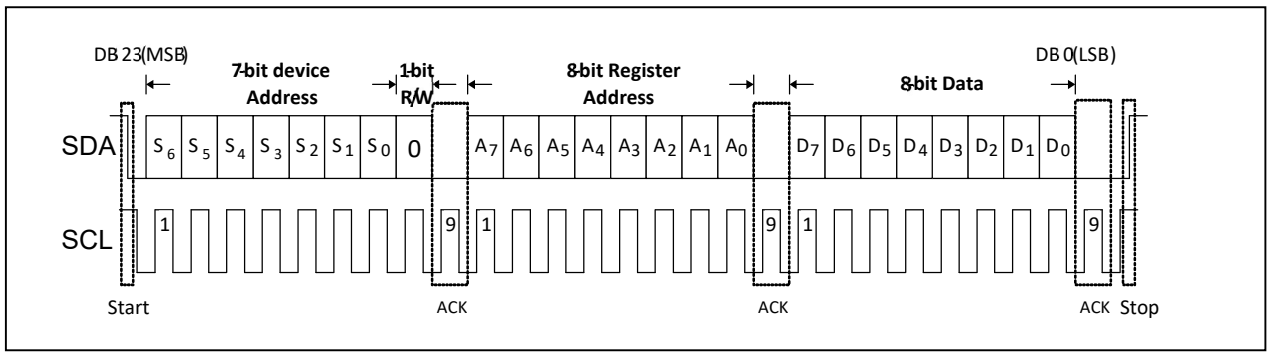


Figure 5: I^{2}C write sequence

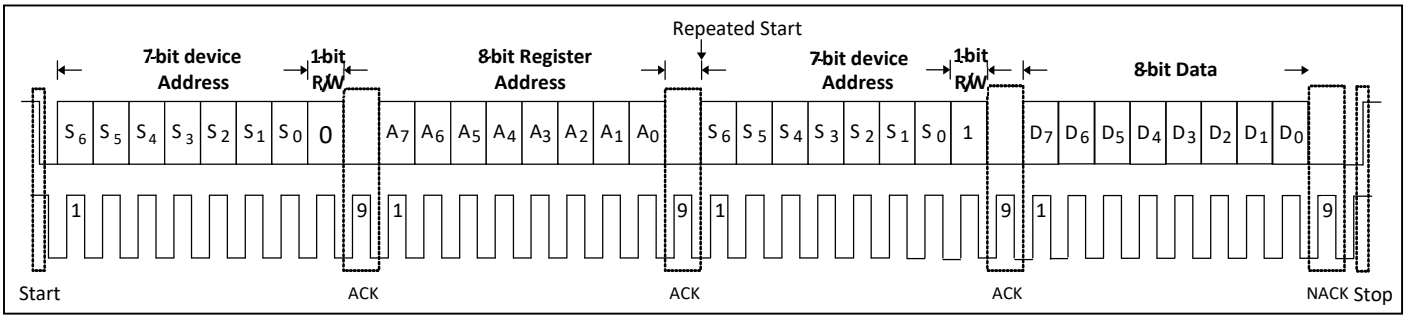


Figure 6: I²C read sequence

APPLICATION NOTE

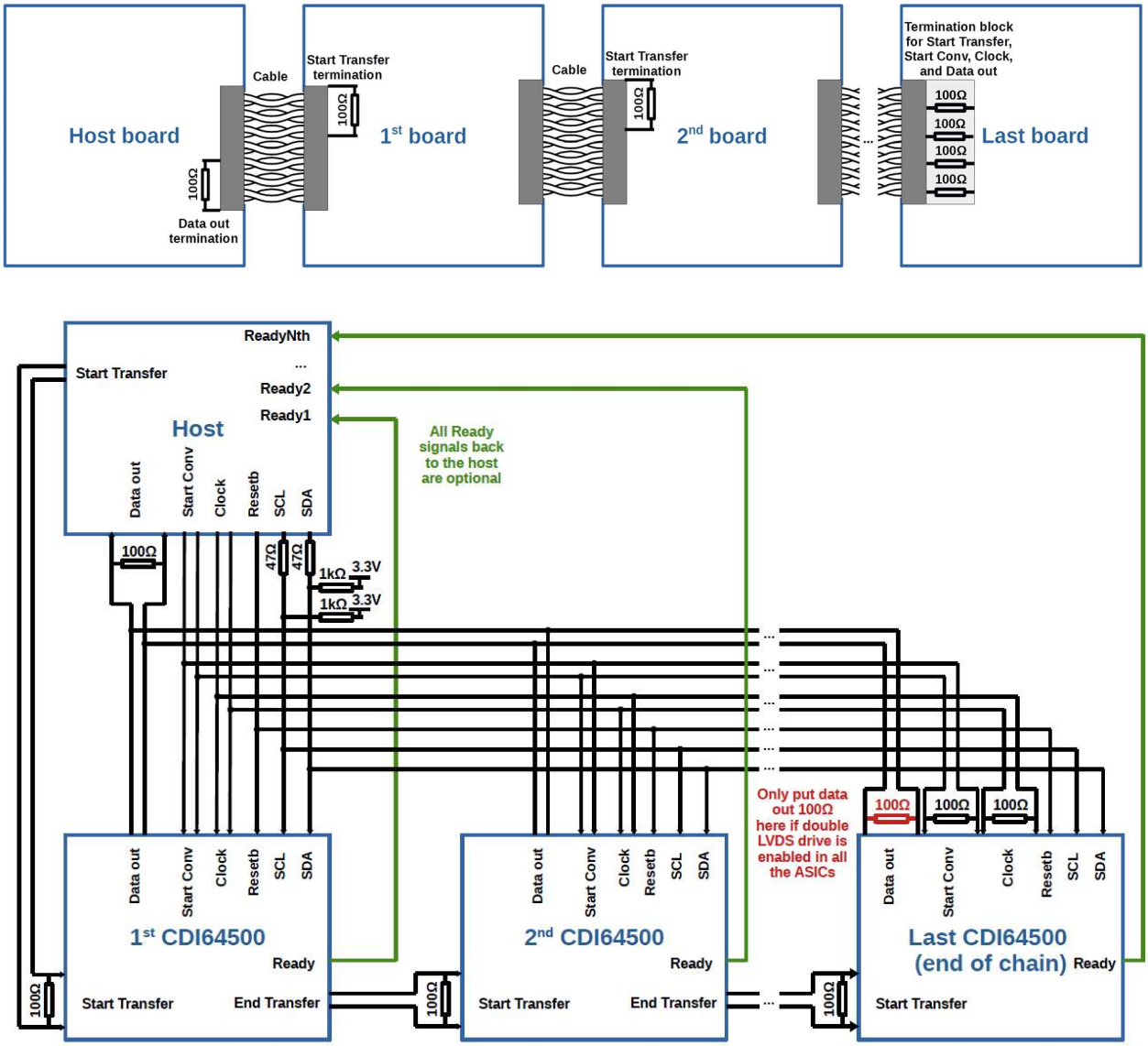


Figure 7: Board level (top) and chip level (bottom) daisy chain diagrams.

The application schematic is illustrated in Figure 1. The daisy chain connections and terminations for multiple chips are shown in Figure 7.

Power supply

- The Analog section operates on minimum 5V power supply, it is recommended to set the VCC to 5.25V.
- The Digital section operates at 3.3V ± 5%.
- Both analog VCC and digital VDD power supplies must be as quiet as possible. It is recommended to use bypass external ceramic capacitors of at least 10µF and use separate linear regulators with PSRR > 60dB for each power supplies.
- It is recommended to connect both analog and digital grounds (AGND and DGND) to a single ground plane on the PCB and use separate low disturbance ground source.
- It is recommended to have a settled clock prior to powering on the ASIC.
- It is recommended to manually reset the ASIC after power on to correctly initialize it. The minimum Resetb pulse-width duration is 1µs.

Analog

- **Vset** pin requires a low impedance, low noise external 4.0V reference voltage. The output noise of this external reference circuit should be less than 10µV rms.
- **Ext_res** pin is connected to GND through to a 6kOhm (± 1%) default resistor used to provide a constant current bias for all internal circuits, so a low temperature coefficient is required (< 50ppm).
- **Ext_res** resistor can be changed to improve noise performance depending on the gain settings. For gain ranges <3pF, the Ext_res resistor can be increased to values as high as 20kohm. For gain ranges >3.5pF, the Ext_res resistor can decrease to value as low as 2kohm.
- **Ramp_out** is directly connected to **Ramp_in.**
- **Test_in** should be tied to AGND, **Test_out** should be left floating.
- For best noise performance, the input channel traces should be shielded and away from digital or noisy signal traces.

Digital

- The recommended operation frequency is 40MHz. Higher frequency (Maximum 68MHz) will reduce conversion time but increase power consumption.
- For CDI64500 to operate correctly, timing table and register settings must be programmed correctly and be valid. Since I2C communication is sensitive to ringing and signal reflection, a 47-ohm series resistor should be added to SDA and SCL between the host and the daisy chain, as shown in Figure 7. It is also recommended to verify the validity of timing table and register settings before starting data acquisition.
- The I2C bus can only be shared with up to 16 CDI64500 devices. The device address of the cascaded devices (through **Start_transfer** and **End_transfer**) will be set after the DAACQU command has been issued by the host. If bit 4 of the device address is set then all devices on the I2C bus will accept write command simultaneously, otherwise only the addressed device will respond to read / write commands.
- In daisy chain applications, the **DATAO** bus can be shared with up to 16 devices. Also, multiple groups of devices can share **Clock**, **Resetb** and **Start_conv**. For such system architecture, care should be provided for the Clock distribution network on the PCB. In double LVDS drive mode, the termination resistor should be placed at **both ends** of the DATAO to remove echo from each end of the busses and bit 7 of RESCTRL should be set to 1 to increase the drive. If there is only one device in the chain, then the termination resistor can be set at the receive end with bit 7 of RESCTRL set to 0.
- The LDVS receivers do not have internal termination resistors, and as such external termination resistors are required. Please refer to Figure 7 for external termination resistor placements.
- The **Test_enable** signal should be tied to DGND.
- For best noise performance, the **Start_Transfer** command should not be issued within 30µs after **Start_Conv** is activated.
- The Ramp gen acquisition speed should be set to “Fast” in RESCTRL register when the ramp time is faster than 150µs.
- In greater than 2 meters long cable communications, a local clock oscillator is recommended on PCB for the system clock.
- In long cable communications, the DATAO can have communication latency delay and cause readout errors. To improve robustness of DATAO, it is recommended to implement a resynchronization for every chip in the chain by using the start bit. To resynchronize at the host, a faster clock, for example, 4 times faster than the system clock, will provide 4 phases where the DATAO can be sampled. During the readout, the host will select the optimal sampling phase for each chip in the chain.

DIE PIN LIST & DESCRIPTIONS

Pad	X-Axis (um)	Y-Axis (um)	Mnemonic	Pad Type	Description
1	62	5381	IN<6>	Analog Input	Charge input Channel 6
2	62	5281	IN<7>	Analog Input	Charge input Channel 7
3	62	5181	IN<8>	Analog Input	Charge input Channel 8
4	62	5081	IN<9>	Analog Input	Charge input Channel 9
5	62	4981	IN<10>	Analog Input	Charge input Channel 10
6	62	4881	IN<11>	Analog Input	Charge input Channel 11
7	62	4781	IN<12>	Analog Input	Charge input Channel 12
8	62	4681	IN<13>	Analog Input	Charge input Channel 13
9	62	4581	IN<14>	Analog Input	Charge input Channel 14
10	62	4481	IN<15>	Analog Input	Charge input Channel 15
11	62	4381	IN<16>	Analog Input	Charge input Channel 16
12	62	4281	IN<17>	Analog Input	Charge input Channel 17
13	62	4181	IN<18>	Analog Input	Charge input Channel 18
14	62	4081	IN<19>	Analog Input	Charge input Channel 19
15	62	3981	IN<20>	Analog Input	Charge input Channel 20
16	62	3881	IN<21>	Analog Input	Charge input Channel 21
17	62	3781	IN<22>	Analog Input	Charge input Channel 22
18	62	3681	IN<23>	Analog Input	Charge input Channel 23
19	62	3581	IN<24>	Analog Input	Charge input Channel 24
20	62	3481	IN<25>	Analog Input	Charge input Channel 25
21	62	3381	IN<26>	Analog Input	Charge input Channel 26
22	62	3281	IN<27>	Analog Input	Charge input Channel 27
23	62	3181	IN<28>	Analog Input	Charge input Channel 28
24	62	3081	IN<29>	Analog Input	Charge input Channel 29
25	62	2981	IN<30>	Analog Input	Charge input Channel 30
26	62	2881	IN<31>	Analog Input	Charge input Channel 31
27	62	2781	IN<32>	Analog Input	Charge input Channel 32
28	62	2681	IN<33>	Analog Input	Charge input Channel 33
29	62	2581	IN<34>	Analog Input	Charge input Channel 34
30	62	2481	IN<35>	Analog Input	Charge input Channel 35
31	62	2381	IN<36>	Analog Input	Charge input Channel 36
32	62	2281	IN<37>	Analog Input	Charge input Channel 37
33	62	2181	IN<38>	Analog Input	Charge input Channel 38
34	62	2081	IN<39>	Analog Input	Charge input Channel 39
35	62	1981	IN<40>	Analog Input	Charge input Channel 40
36	62	1881	IN<41>	Analog Input	Charge input Channel 41
37	62	1781	IN<42>	Analog Input	Charge input Channel 42
38	62	1681	IN<43>	Analog Input	Charge input Channel 43
39	62	1581	IN<44>	Analog Input	Charge input Channel 44
40	62	1481	IN<45>	Analog Input	Charge input Channel 45
41	62	1381	IN<46>	Analog Input	Charge input Channel 46
42	62	1281	IN<47>	Analog Input	Charge input Channel 47
43	62	1181	IN<48>	Analog Input	Charge input Channel 48
44	62	1081	IN<49>	Analog Input	Charge input Channel 49
45	62	981	IN<50>	Analog Input	Charge input Channel 50
46	62	881	IN<51>	Analog Input	Charge input Channel 51
47	62	781	IN<52>	Analog Input	Charge input Channel 52
48	62	681	IN<53>	Analog Input	Charge input Channel 53
49	62	581	IN<54>	Analog Input	Charge input Channel 54
50	62	481	IN<55>	Analog Input	Charge input Channel 55
51	62	381	IN<56>	Analog Input	Charge input Channel 56
52	62	281	IN<57>	Analog Input	Charge input Channel 57
53	239	62	IN<58>	Analog Input	Charge input Channel 58
54	339	62	IN<59>	Analog Input	Charge input Channel 59

Pad	X-Axis (um)	Y-Axis (um)	Mnemonic	Pad Type	Description
55	439	62	IN<60>	Analog Input	Charge input Channel 60
56	539	62	IN<61>	Analog Input	Charge input Channel 61
57	639	62	IN<62>	Analog Input	Charge input Channel 62
58	739	62	IN<63>	Analog Input	Charge input Channel 63
59	874	100	AGND	Ground	Analog Ground
60	1084	100	VSET	Analog Input	4V low noise reference input
61	1294	100	VCC	Power	5V analog power supply
62	1504	100	RAMP_OUT	Analog Output	Internal ramp generator output
63	1714	100	RAMP_IN	Analog Input	Ramp input for comparator
64	1924	100	TEST_OUT	Analog Output	Test output
65	2134	100	VCC	Power	5V analog power supply
66	2344	100	AGND	Ground	Analog Ground
67	2805	105	TEST_ENABLE	Digital Input	Test enable (for production test; should be tied low for normal operation)
68	3008	105	DGND	Ground	Digital Ground
69	3211	105	VDD	Power	3.3V digital power supply
70	3414	105	READY	Digital Output	Data is ready
71	3617	105	RESETB	Digital Input	Digital reset pin
72	3882	412	START_CONVN	LVDS Input	Start conversion
73	3882	643	START_CONVP		
74	3882	807	START_TRANSFERN	LVDS Input	Start data transfer from ASIC
75	3882	1039	START_TRANSFERP		
76	3882	1203	CLKN	LVDS Input	System clock (30MHz – 68MHz)
77	3882	1435	CLKP		
78	3882	1608	DGND	Ground	Digital Ground
79	3882	4121	VDD	Power	3.3V digital power supply
80	3882	4294	END_TRANSFERN	LVDS Output	Signal End of data transfer
81	3882	4679	END_TRANSFERP		
82	3882	4844	DATAON	LVDS Output	Data out LVDS pair. Drive controlled by bit 7 of register RESCTRL
83	3882	5229	DATAOP		
84	3625	5535	SDA	Open Drain I/O	I2C data line
85	3414	5535	SCL	Digital Input	I2C clock line
86	3211	5535	VDD	Power	3.3V digital power supply
87	3008	5535	DGND	Ground	Digital Ground
88	2384	5541	AGND	Ground	Analog Ground
89	2174	5541	VCC	Power	5V analog power supply
90	1964	5541	TEST_IN	Analog Input	Test input, use this input to inject current into selected channel
91	1754	5541	EXT_RES	Analog Input	External bias resistor (use 5.9k to ground)
92	1544	5541	VCC	Power	5V analog power supply
93	1334	5541	AGND	Ground	Analog Ground
94	1124	5541	VSET	Analog Input	4V low noise reference input
95	914	5541	ZERO	Analog Input	Common positive input of the amplifier
96	739	5577	IN<0>	Analog Input	Charge input Channel 0
97	639	5577	IN<1>	Analog Input	Charge input Channel 1
98	539	5577	IN<2>	Analog Input	Charge input Channel 2
99	439	5577	IN<3>	Analog Input	Charge input Channel 3
100	339	5577	IN<4>	Analog Input	Charge input Channel 4
101	239	5577	IN<5>	Analog Input	Charge input Channel 5

DIE OUTLINE

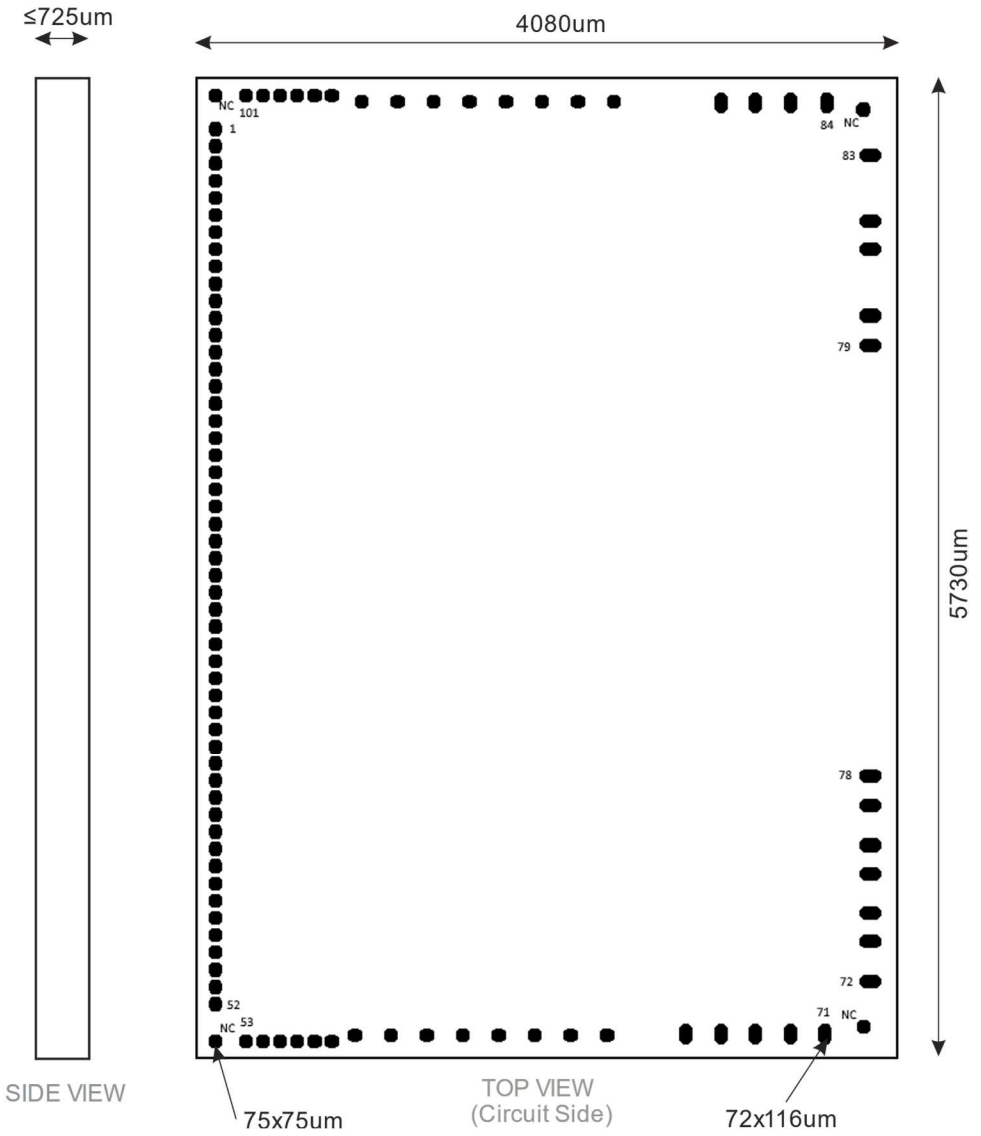
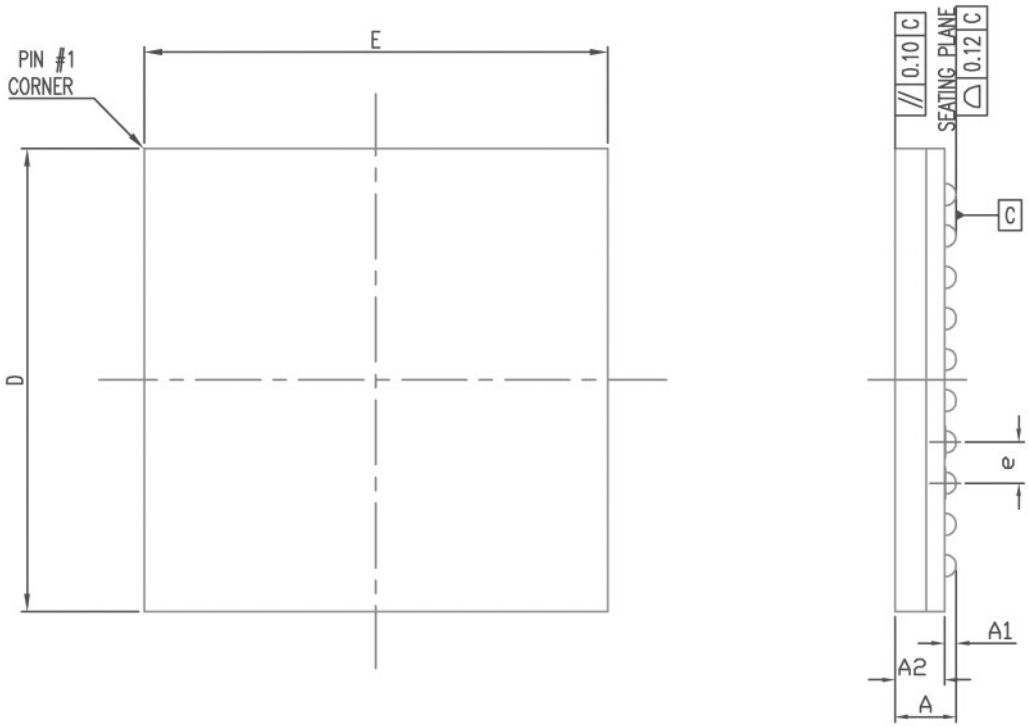


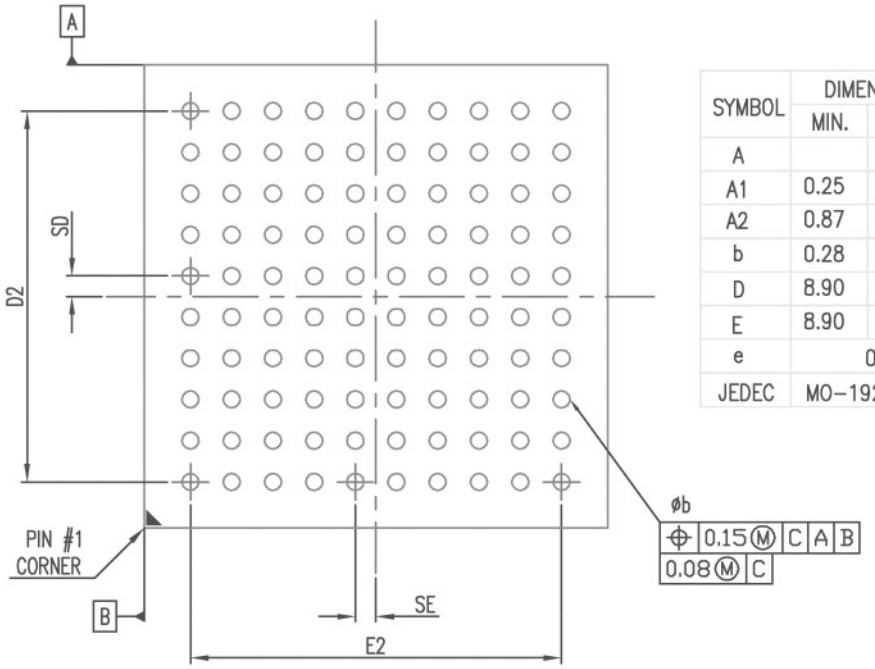
Figure 8: Bare Die

DIE SPECIFICATIONS

Parameter	Value	Unit
Die Size	4080 x 5730	um
Bond Pad Composition	AlCu (0.5% Cu)	
Bond Pad Sizes	75 x 75 72 x 116	um
Passivation Type	SiO2/Si3N4	
Thickness	≤725	um
Backside Bias	Ground	
Scribe (Street) Width	90 x 90	um

fpBGA PACKAGE DESCRIPTION





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A		1.19	1.33		0.047	0.052
A1	0.25	0.30		0.007	0.009	
A2	0.87	0.96		0.034	0.038	
b	0.28	0.33	0.38	0.011	0.013	0.015
D	8.90	9.00	9.10	0.350	0.354	0.358
E	8.90	9.00	9.10	0.350	0.354	0.358
e	0.80 BSC.			0.031 BSC.		
JEDEC	MO-192,205					

N	SE (mm)	SD (mm)	E2(mm)	D2(mm)	JEDEC(REF)
100	0.40 BSC.	0.40 BSC.	7.20 BSC.	7.20 BSC.	

Ball count: 100; Ball pitch: 0.8 mm; Bond type: Au Ball; Ball size: 460um; Ball material: Lead-free

fpBGA PIN CONFIGURATION

Top View

	A	B	C	D	E	F	G	H	J	K
1	*ZERO*	*CH05*	*CH04*	*CH03*	*CH02*	*CH01*	*CH00*	*EXT_RES*	*SCL*	*DATAOP*
2	*CH11*	*CH08*	*CH06*	*CH07*	*CH09*	*CH10*	*CH12*	*VCC*	*SDA*	*DATAON*
3	*CH17*	*CH15*	*CH13*	*CH14*	*CH16*	*CH18*	*CH19*	*TEST_IN*	*VDD*	*END_TRANSFERP*
4	*CH24*	*CH22*	*CH21*	*CH20*	*CH23*	*CH25*	*VSET*	*AGND*	*DGND*	*END_TRANSFERN*
5	*CH29*	*CH26*	*CH28*	*CH27*	*CH30*	*CH31*	*AGND*	*AGND*	*DGND*	*CLKP*
6	*CH34*	*CH37*	*CH35*	*CH36*	*CH33*	*CH32*	*AGND*	*AGND*	*DGND*	*CLKN*
7	*CH39*	*CH41*	*CH42*	*CH43*	*CH40*	*CH38*	*VSET*	*TEST_OUT*	*VDD*	*START_TRANSFERP*
8	*CH46*	*CH48*	*CH50*	*CH49*	*CH47*	*CH45*	*CH44*	*VCC*	*TEST_EN*	*START_TRANSFERN*
9	*CH52*	*CH55*	*CH57*	*CH56*	*CH54*	*CH53*	*CH51*	*RAMP_OUT*	*READY*	*START_CONVP*
10	*ZERO*	*CH58*	*CH59*	*CH60*	*CH61*	*CH62*	*CH63*	*RAMP_IN*	*RESETB*	*START_CONVN*

fpBGA Package
100-Lead, 10x10 array, 9mm x 9mm

PIN LIST

Pin index	Pin count	Name	Type	Purpose
	64	IN0-IN63	Analog Input	Charge input
A1, A10	2	Zero	Analog Input	Common positive input of the amplifier
H1	1	Ext_res	Analog Input	Bias resistor use 5.9k to ground
G4, G7	2	Vset	Analog Input	4V low noise reference input
H9	1	Ramp_out	Analog Output	Internal ramp generator output
H10	1	Ramp_in	Analog Output	Ramp input for comparator
H3	1	Test_in	Analog Input	Test input, use this input to inject current into selected channel
H7	1	Test_out	Analog Output	Test output
J8	1	Test_enable	Input	Test enable (for production test; should be tied low for normal operation)
H2, H8	2	VCC	Power	5V analog power supply
G5, G6, H4-H6	5	AGND	Ground	Analog ground
K1, K2	2	DATAO+/-	LVDS Output	Data out LVDS pair. Drive controlled by bit 7 of register RESCTRL.
K9, K10	2	START_CONV+/-	LVDS Input	Start conversion
K7, K8	2	START_TRANSFER+/-	LVDS Input	Start data transfer from ASIC
K3, K4	2	END_TRANSFER+/-	LVDS Output	Signal End of data transfer
J9	1	Ready	Output	Data is ready
K5, K6	2	CLOCK+/-	LVDS IN	System clock (30MHz to 68MHz)
J2	1	SDA	Open Drain I/O	I2C data line
J1	1	SCL	Input	I2C clock line
J3, J7	2	VDD	Power	3.3V digital power supply
J4-J6	3	DGND	Ground	Digital ground
J10	1	Resetb	Input	Digital reset pin
Total	100			

ORDERING GUIDE

Model[1]	Operating Temperature	Package Description	MSL Peak Temp[2]
CDI64500[1]	-20°C to 80°C	fpBGA	Level-3-260C-168 HR
CDI64500-KGD	-20°C to 80°C	Bare Die	-
CDI64500-WAFER	-20°C to 80°C	Bare Die Wafer	-

[1] All models are RoHS compliant part.
[2] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

REVISION HISTORY

REV	DATE	DESCRIPTION
A	06/14	Preliminary release
B	02/15	Update for chip rev2.0 Added die and wafer info. Added User Programmable Feature section.
C	11/17	Update Conversion Clock. Added Application Information. Remove Watermark.
D	01/18	Added RoHS compliant part.
E	03/18	Added MSL peak temp.
F	04/18	Added BGA ball descriptions
G	04/18	Default value of LVDS drive is 3mA (register value 0) and the general broadcast address is 0x10
H	06/18	Test purpose status bits reserve, added power on recommendations in application notes, fixed maximum clock frequency in pin description, fixed default value in timing table.
I	07/18	Change maximum frame rate table and timing table formulas and descriptions.
J	10/18	Change in LVDS settling clock cycle and I2C descriptions.
K	1/19	Ext_res values to optimize noise, application note error i2c share device, lvds double drive for data out only.
L	2/19	Added Daisy chain diagrams, I2C read diagram, SCL 1kohm pull-up, and changed bare die and scribe seal dimensions.
M	5/19	Added system clock range from 30MHz to 68MHz.
N	10/19	Added register h82 phase generator and duty cycle locks descriptions.
O	11/19	Change application.
P	04/20	Add information about min Resetb pulse-width and min delay between Resetb and first Start_Conv. Updated Figure 1.
Q	07/21	Removed maximum frame rate in features of the chip
R	04/22	Removed RESCTRL register h81 “abort current frame” and updated register h82 table and description. Added new application notes for power, analog and digital.
S	03/23	Change in application note. Added series resistors for I2C lines to improve signal integrity.
T	08/23	I2C lines must be dedicated and reserved for CDI64500