CDI12100

12-Channels Sensor Analog Front End

FEATURES

- 12 amplifier, rectifier and filter channels
- Carrier output signal (CLK/128) used to drive the excitation source
- Built-in phase detector and rectifier
- Accepts internal or external rectified signal
- 14 programmable gains (27dB -> 93dB)
- Good matching between filters (<1%)
- Adjustable filter frequency and bandwidth using external clock (250kHz - 4MHz)
- Operates at up to +/- 10V power supply
- Low power (< 240mW overall power dissipation [20mW/channel])

DESCRIPTION

The CDI12100 is composed of 12 channels, each containing an amplifier, a rectifier and a filter.
The CDI12100 is available in a 48pin 6x6mm QFN.

APPLICATIONS

- Security metal detection
- Proximity detection

FUNCTIONAL BLOCK DIAGRAM

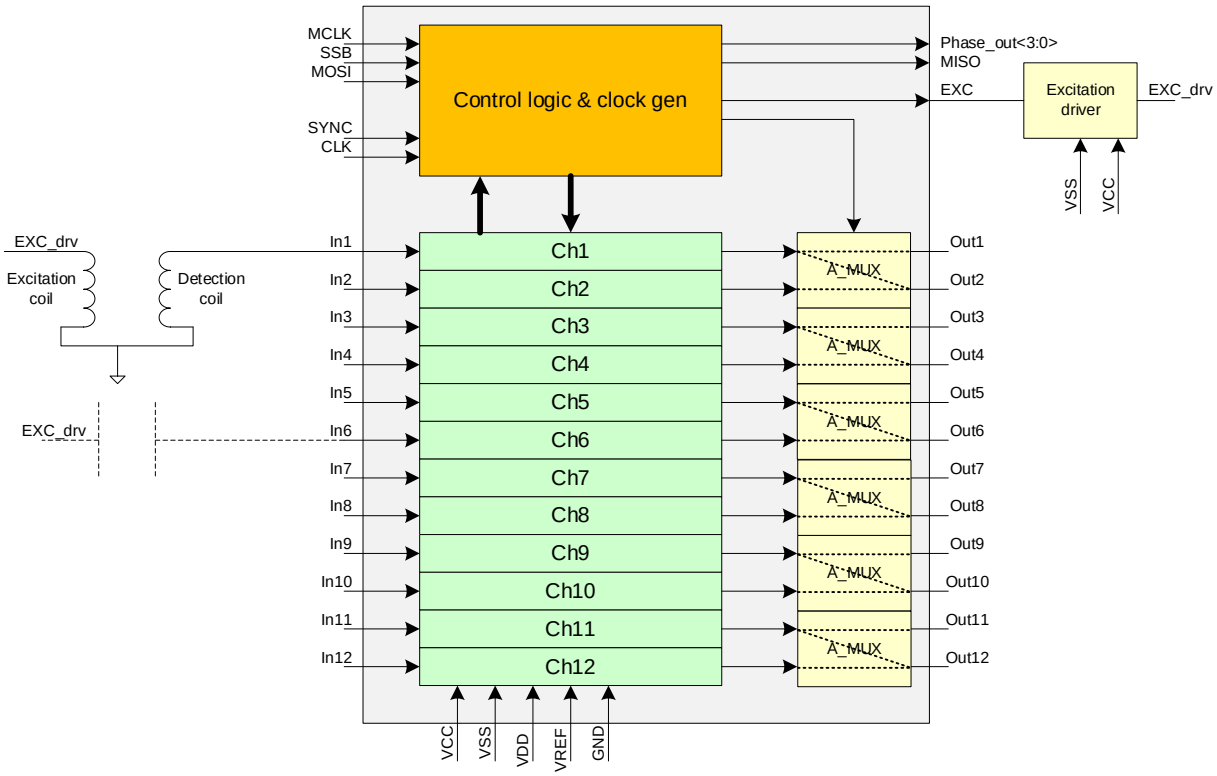

Figure 1.

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Tel: 514-340-1550 www.comport-data.com
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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	*Max*	
Positive Power Supply Voltage	VCC		12	V
Negative Power Supply Voltage	VSS		-12	V
Low Voltage Power supply (Digital)	VDD		6.0	V
All input (Analog)		VSS-0.3	VCC+0.3	V
All input (Digital)		-0.3	VDD+0.3	V
Storage Temperature	TSTG	-50	150	°C
Operating Temperature Range	Tamb	-20	85	°C
Lead Temperature (soldering, 10 seconds)	TL		220	°C
ESD HBM Protection on all pin (except inpit)	Vesd		1.5	kV

ELECTRICAL CHARACTERISTICS

Power supply Voltages and Current

Parameter description / test conditions	Minimum	Typical	Maximum	Unit
Power supply voltage VCC	5	8	10	V
Power supply voltage VSS	-5	-8	-10	V
Power supply voltage VDD	3.0	5.0	5.5	V
Operation mode current VCC		9	15	mA
Operation mode current VSS		9	15	mA
Operation mode current VDD		8	13	mA
Power consumption per channel (+/-8V)		18	25	mW/ch

Reference clock

Parameter description / test conditions	Minimum	Typical	Maximum	Unit
Input clock (CLK)	200	1000	4000	KHz

First stage carrier bandpass filter and amplifier

Parameter description / test conditions	Minimum	Typical	Maximum	Unit
Analog Input range	VSS		VCC	V
Central frequency		8		K Hz
Bandwidth (-3dB)	3		18	K Hz
Programmable Gain (8kHz input signal)	24		32	dB

Rectifier stage bandpass filter and amplifier

Parameter description / test conditions	Minimum	Typical	Maximum	Unit
Analog Input range	VSS		VCC	V
Central frequency (1MHz input clock)		1.5		Hz
Bandwidth (-3dB)	0.5		4	Hz
Programmable Gain (1 Hz input signal)	30		42	dB

Low voltage bandpass filter amplifier

Parameter description / test conditions	Minimum	Typical	Maximum	Unit
Analog Input range	VSS		VCC	V
Central frequency (1MHz input clock)		1.5		Hz
Bandwidth (-3dB)	0.5		4	Hz
Fixed Gain (1 Hz input signal)	0		30	dB

Noise performance

Parameter description / test conditions	Minimum	Typical	Maximum	Unit
Output noise at maximum gain (93dB)		4		mV_{rms}
Output noise at typical gain (87dB)		2		mV_{rms}

TIMING SPECIFICATIONS

SPI interface timing

Parameter description	Symbol	Minimum	Typical	Maximum	Unit
MCLK clock period	Tcp			25	MHz
Setup time from SSb low to SCLK high	Tsc	100			ns
Hold time from SSb high to MCLK low	Thc	100			ns
MOSI setup time to MCLK rising	Tsi	5			ns
MOSI Hold time to MCLK rising	Thi	3			ns
MISO propagation time from MCLK falling	Tdo			8	ns

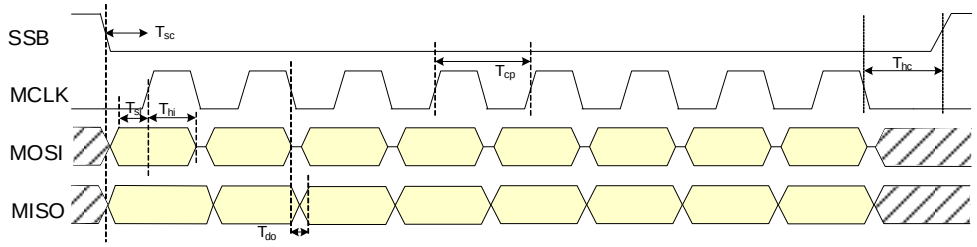


Figure 2: SPI timing (CPOL = 0 / CPHA = 0)

Note: MISO is not high-impedance when SSB goes high, so this device cannot share the SPI communication link with other devices.

FUNCTIONALITY

The channel is designed for low frequency carrier demodulation and amplification (input ~ 4-20kHz, output 0.5Hz-2Hz, 93dB gain) application. The channel is composed of seven sub-blocks, as follows:

- High voltage Carrier amplifier and band-pass filter.
- High voltage Phase detector.
- High voltage Full wave rectifier. The signal from the carrier filter will be demodulated using internal/external demodulator signal.
- Baseband bandpass filter. The demodulated signal is translated into the 0-3.3V power supply domain.
- Lowpass filter, the signal from first bandpass filter will be amplified and filtered.
- Second bandpass filter, the signal is filtered by the final bandpass filter to overcome all interference and noise components.
- Output mux and buffer. A multiplexer followed by a buffer allows the user to select the output of each gain block. The carrier signal can be also selected but it has a gain of -20dB.

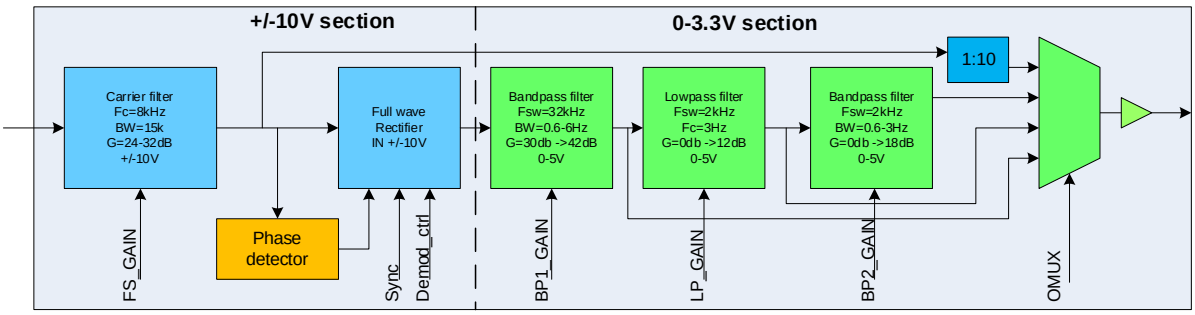


Figure 3: Channel block diagram

Note: All the frequency responses are based on the input 1MHz. User can change input clock frequency to fit their application requirement.

CARRIER FILTER AND AMPLIFIER

The first stage is a bandpass filter/amplifier, it is used to amplify the carrier signal at 1/128 of CLK. The high voltage output range (~20V_{pp}) will improve the sensitivity of the system.

- Lower corner 1.5kHz
- Upper corner 30kHz
- Center frequency 8kHz
- Selectable gain from 23dB to 32dB in three 3dB steps (***FS_GAIN*** register)
- Input signal range: +/- 1V
- Output signal range: +/-10V.

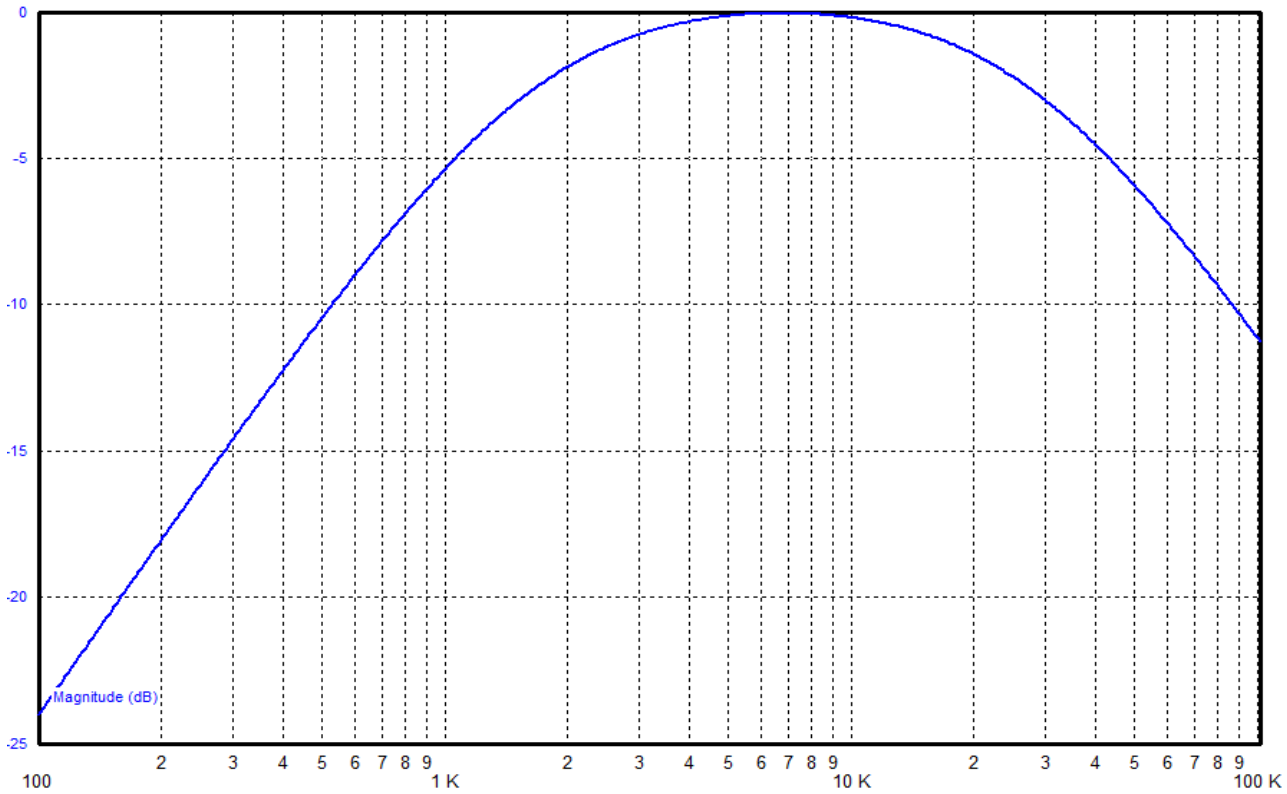


Figure 4: First stage frequency response

PHASE DETECTOR & OUTPUT LOGIC

The phase detector detects the cross over location of the carrier signal, the output of this circuit is used in the rectifier to demodulate the carrier.

- Phase detector circuit compares the output of the carrier filter stage with ground node, it will output 1 when signal greater than 0 and vice versa.
- The phase output of the 12 channels is routed through 4 groups of 3 channels each (Phase_out<3:0>).
- The register ***Ch_phase_sel***<1:0> is to select which of the four channel groups are seen on the Phase_out signals. See table in SPI registers section.
- The “Phase_out” signal will be gated with “Sync” signal when “***Phase_ctrl***” is one. (Phase_out = Phase_in & Sync)
- The phase detector is synchronized with the main clock signal.

RECTIFIER

The rectifier takes AC signal from the carrier bandpass and then rectifies it to remove the carrier component.

- The rectifier demodulates the carrier frequency into base band frequency. The rectifier signal source can be from internal phase detector (***Demod_ctrl***=0) or external source ("SYNC") when ***Demod_ctrl***=1.
- The rectifier is a full wave rectifier when both halves of the signal are used.

FIRST BANDPASS FILTER AND AMPLIFIER

Base band filter takes the signal from the rectifier and reduces the signal bandwidth down to 1.5Hz range:

- Center frequency 1.5Hz
- Lower corner 0.5Hz
- Upper corner 3.2Hz
- Attenuation at carrier frequency ~-40dB
- Selectable gain from 30dB to 42dB in 6dB step
- Input signal range: +/- 10V
- Output signal range: 0V-3.3V centered at Vref.

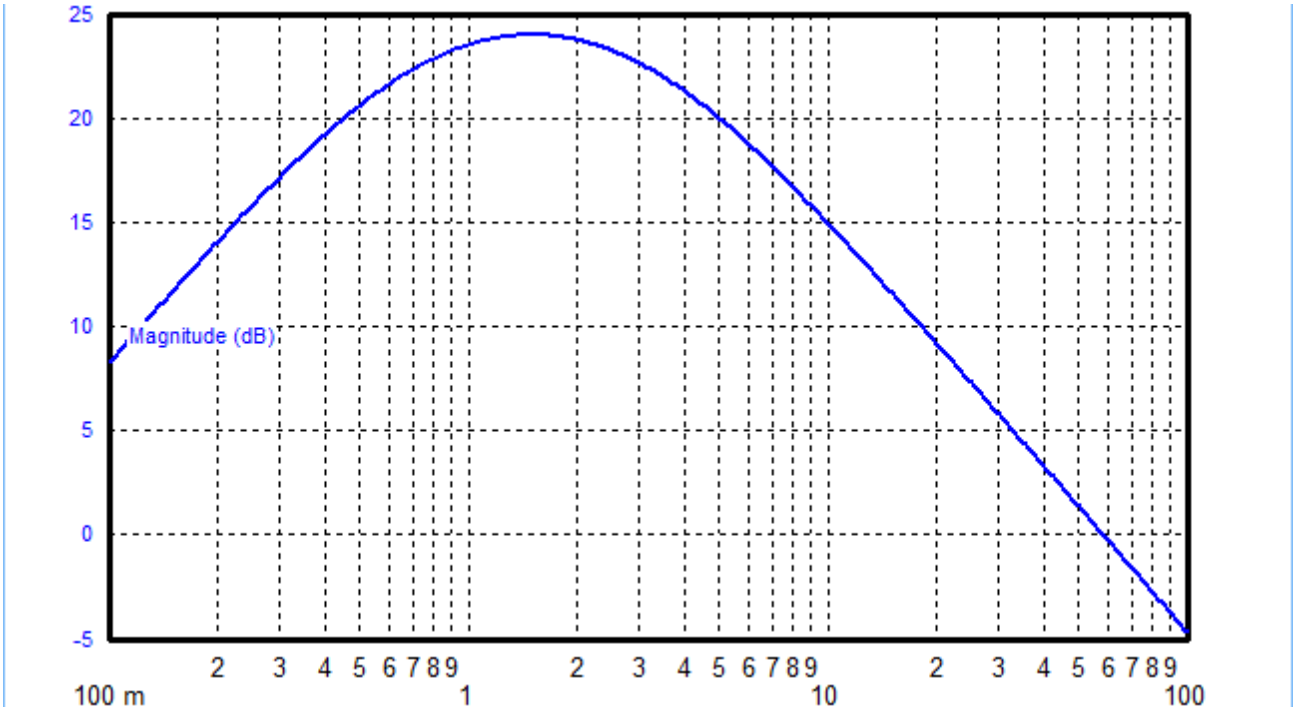


Figure 5: First bandpass filter AC response

LOW PASS FILTER AND AMPLIFIER

The low pass filter takes the signal from the rectifier and reduces the signal bandwidth down to 3Hz range:

- First order filter
- Upper corner 3Hz
- Selectable gain from 0dB to 12dB in two 6dB step (***LP_GAIN*** register)
- Input/output signal range: 0V-3.3V

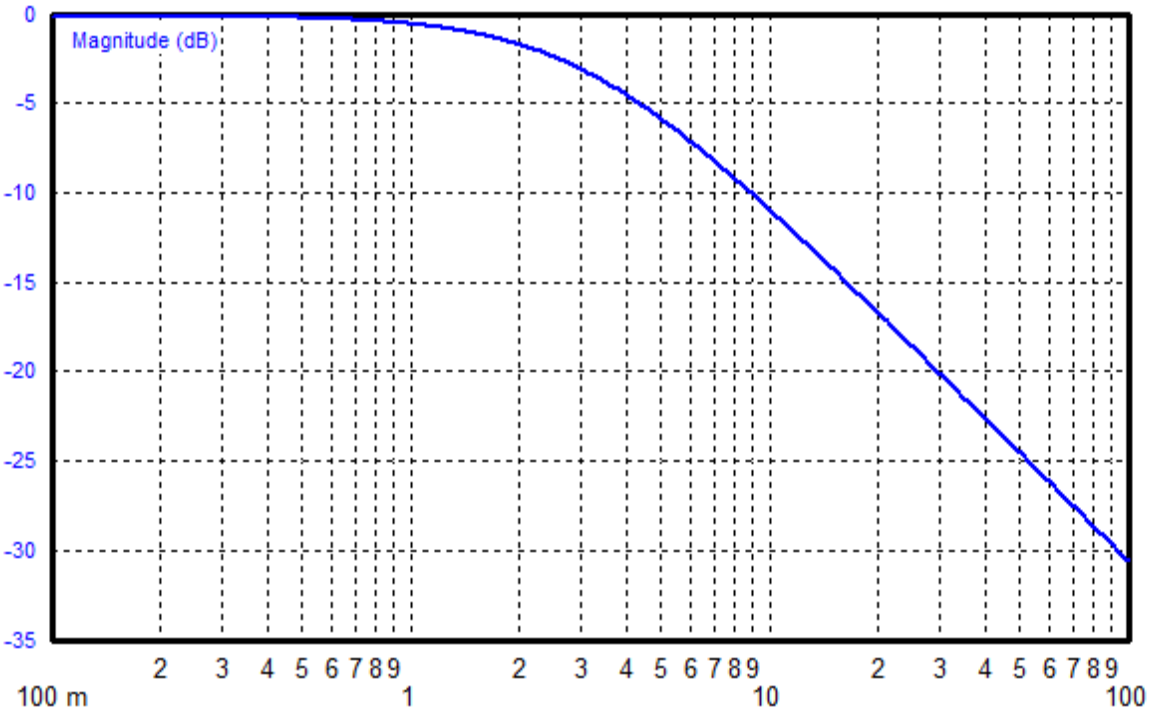


Figure 6: Low pass filter AC response

SECOND BANDPASS FILTER AND AMPLIFIER

This last stage filters and amplifies the output signal from the lowpass filter. Any offset due to the previous high gain stage will also be removed.

- Center frequency 1.5Hz
- Lower corner 0.9Hz
- Upper corner 4.2Hz
- Selectable gain -6dB / 0dB and 6dB
- Input/output signal range: 0V-3.3V

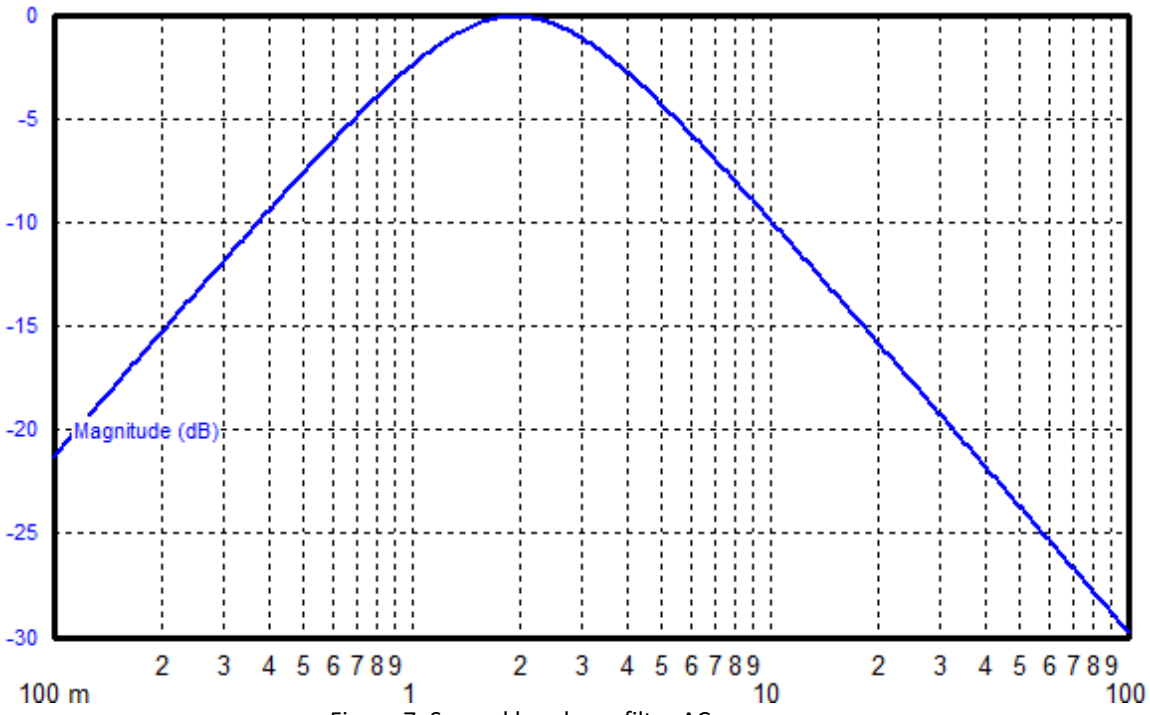


Figure 7: Second bandpass filter AC response

CHANNEL MULTIPLEXER

Sometimes, the dynamic range of the real signal exceeds the output range of the channel, requiring a manual gain reduction that will increase the detection speed due to additional settling time. Therefore, to improve the detection time while keeping the maximum sensitivity, the outputs of all stages will be available at all times using the channel multiplexers. The channel multiplexer followed by a unity gain buffer allows the user to route these signals to the channel output:

- Carrier filter output. Due to limited output range of the output buffer (0-3.3V), this signal is divided by 10 and centered to Vref.
- First bandpass filter.
- Lowpass filter.
- Second bandpass filter.
- Controlled by the ***OMUX*** register, by default the Second bandpass filter is selected.

6 OR 12 CHANNEL OUTPUT MULTIPLEXERS

When the external host ADC has only 8 inputs, the channel multiplexers will allow the user to connect the 12 output channels to 6 physical output pads. In this mode, the host will connect to channels 2, 4, 6, 8, 10 and 12. When the "***Ch_map***" bit is active, the output of the channels 1, 3, 5, 7, 9 and 11 will appear respectively on output of channels 2, 4, 6, 8, 10 and 12.

FAST SETTLING SWITCH

A dedicated "***Fast***" bit allows the user to increase the frequency response of the filter up to 16 times the base frequency. In this mode, the frequency response of the rectifier, base band amplifier and output low voltage amplifier is increased from 1Hz to 16Hz. Setting this pin high for 20ms – 50ms after a gain change or on start up will reduce the settling time of the filter.

DIGITAL INTERFACE

The SPI interface allows the user to program the internal gain and multiplexer setting. The bit map of the 16-bit configuration register is detailed below.

The SPI interface uses the SPI communication protocol with $\mathbf{C_{pol} = 0}$ and $\mathbf{C_{pha} = 0}$, ie: the data is setup at falling edge, captured at rising edge, with the clock idle low.

To update the configuration register, the Host needs to drive 16 clock pulses on MCLK while the chip enable SSB control line is active low, while complying with the timing requirements defined in the electrical characteristics section above. At the end of those 16 clock periods the internal configuration register is updated. While the new programming data is shifted on the MOSI serial data input LSB first, the previous contents of the configuration register are sent to the Host through the serial data output MISO, again LSB first.

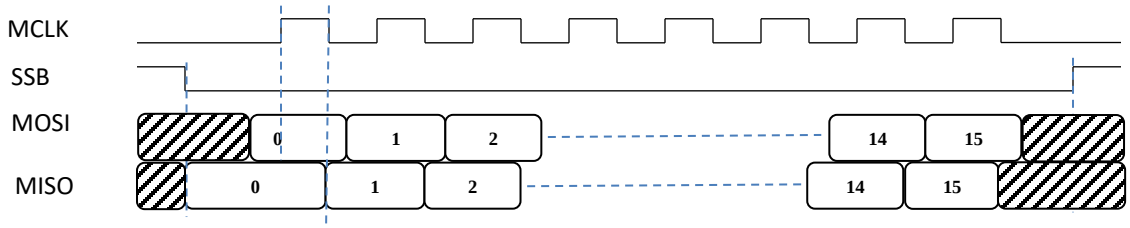


Figure 8: SPI interface timing diagram

SPI REGISTERS

SPI Registers

<table>
<tr><th>Name</th><th>Bit</th><th>Description</th><th>Default</th></tr>
<tr><td>FS_GAIN</td><td>1:0</td><td>Control gain of carrier filter & gain stage
0->23 dB
1->26dB
2->29dB
3->32dB</td><td>0</td></tr>
<tr><td>BP1_GAIN</td><td>3:2</td><td>Control gain of first bandpass filter & gain stage
0->30dB
1->36dB
2->42dB</td><td>0</td></tr>
<tr><td>LP_GAIN</td><td>5:4</td><td>Control gain of low pass & gain stage
0-> 0dB
1-> 6dB
2-> 12dB</td><td>0</td></tr>
<tr><td>BP2_GAIN</td><td>7:6</td><td>Control gain of second bandpass & gain stage
0-> 0dB
1-> 6dB
2-> 12dB
3-> 18dB</td><td>0</td></tr>
<tr><td>OMUX</td><td>9:8</td><td>Channel output select
0 -> Output of second Bandpass filter
1 -> Output of Lowpass filter
2 -> Output of first Bandpass filter
3 -> Output of Carrier filter /10</td><td>0</td></tr>
<tr><td>Demod_ctrl</td><td>10</td><td>Selection between internal demodulation and external demodulator (Sync)
0 -> Internal (Comparator)
1-> External (Sync)</td><td>0</td></tr>
<tr><td>Phase_ctrl</td><td>11</td><td>Control phase output mode
0-> Direct phase comparator output
1-> Comparator & Sync</td><td>0</td></tr>
<tr><td>Ch_phase_sel</td><td>13:12</td><td>Select which channel phase output will be at the phase_out<0:3> signals
<table>
<tr><th>Ch_phase_sel</th><th>phase_out0</th><th>phase_out1</th><th>phase_out2</th><th>phase_out3</th></tr>
<tr><td>0</td><td>Channel 1</td><td>Channel 2</td><td>Channel 7</td><td>Channel 8</td></tr>
<tr><td>1</td><td>Channel 3</td><td>Channel 4</td><td>Channel 9</td><td>Channel 10</td></tr>
<tr><td>2</td><td>Channel 5</td><td>Channel 6</td><td>Channel 11</td><td>Channel 12</td></tr>
<tr><td>3</td><td colspan="4">Reserved</td></tr>
</table></td><td>0</td></tr>
<tr><td>Ch_map</td><td>14</td><td>Select which channel output will be at the even channels
0-> Even channels
1-> Odd channels
<table>
<tr><th>Ch_map</th><th>Odd Channels (1,3,5,7,9,11)</th><th>Even Channels (2,4,6,8,10,12)</th></tr>
<tr><td>0</td><td>Odd Channels</td><td>Even Channels</td></tr>
<tr><td>1</td><td>Odd Channels</td><td>Odd Channels (i.e. ch1 output appears on ch2 output)</td></tr>
</table></td><td>0</td></tr>
<tr><td>Fast</td><td>15</td><td>Increase filter response by a factor of 16 for fast settling time.
0 -> Normal response
1-> 16x</td><td>0</td></tr>
</table>

TYPICAL CONNECTION DIAGRAM

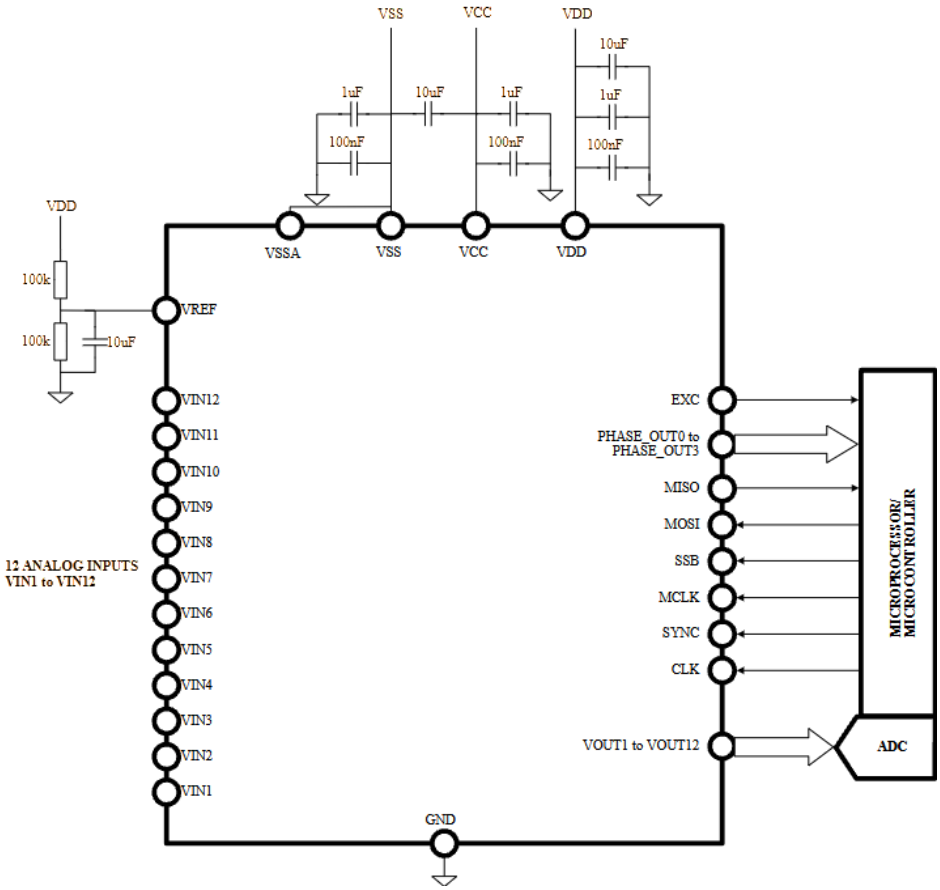
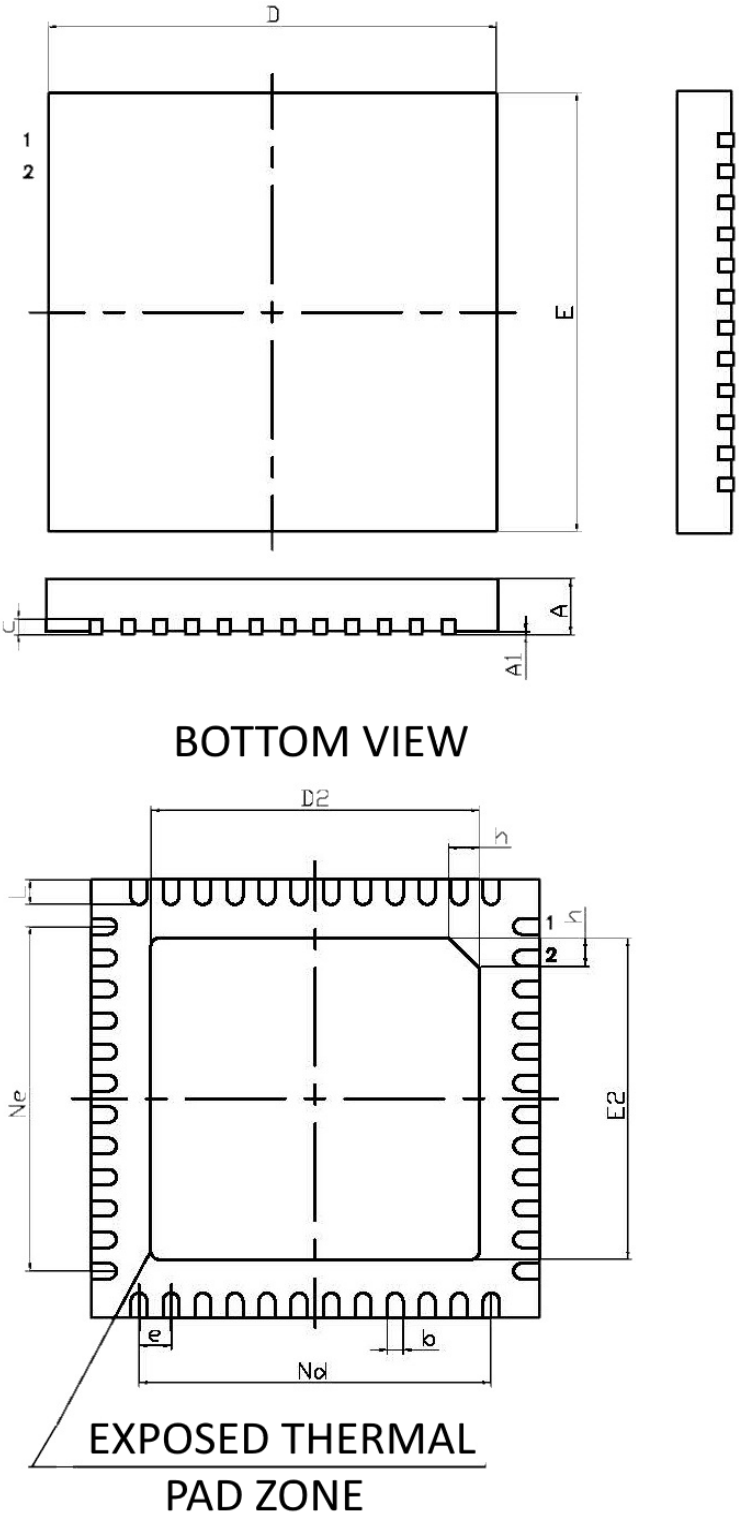


Figure 9: Typical Connection Diagram

PACKAGE MECHANICAL DRAWING



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.02	0. 05
b	0. 15	0.20	0. 25
c	0. 18	0.20	0. 23
D	5. 90	6. 00	6. 10
D2	4. 10	4.20	4. 30
e	0. 40BSC		
Ne	4. 40BSC		
Nd	4. 40BSC		
E	5. 90	6. 00	6. 10
E2	4. 10	4.20	4. 30
L	0. 35	0.40	0. 45
h	0. 30	0. 35	0. 40

Figure 10: QFN Mechanical Drawing

QFN PIN CONFIGURATION

Top View

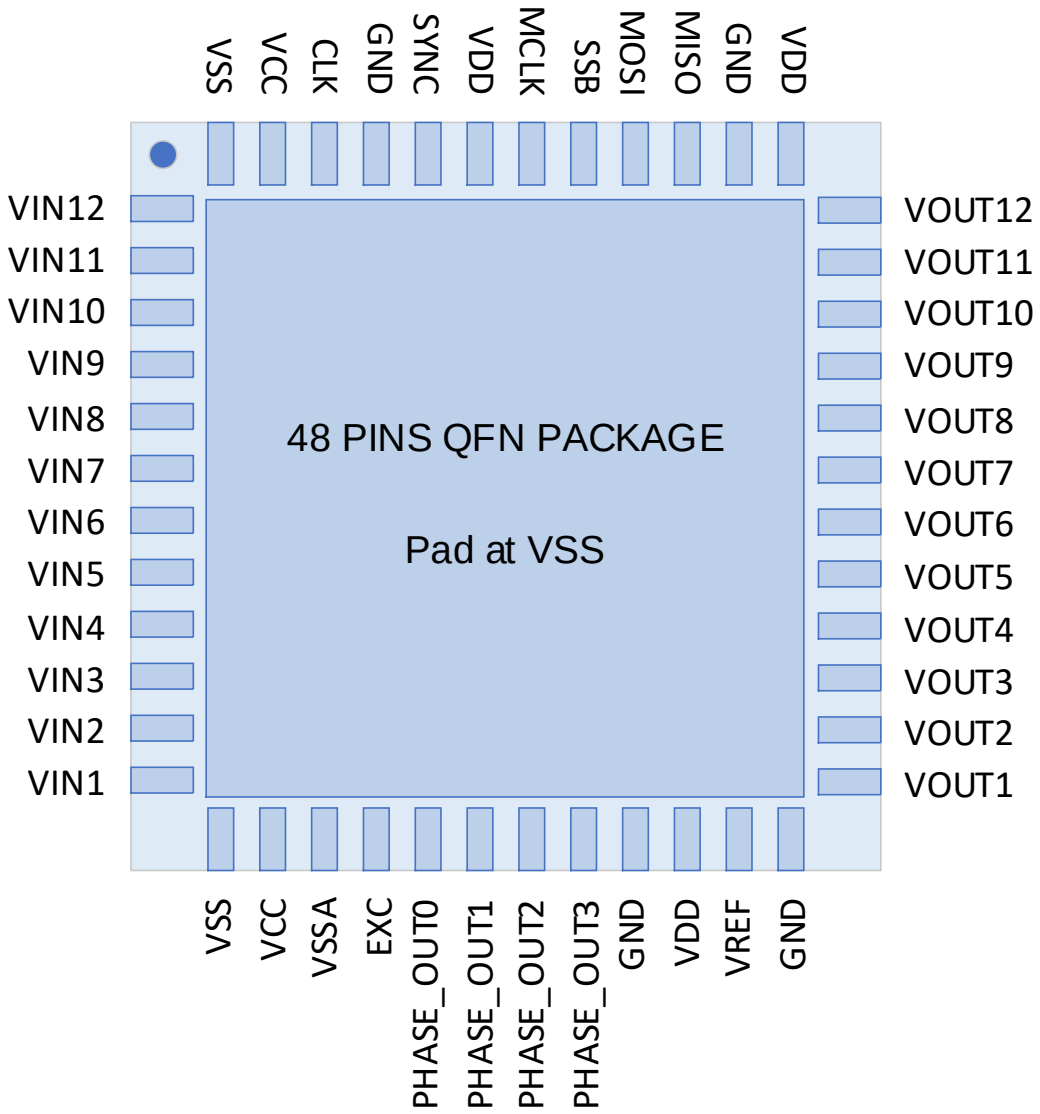


Figure 11: Pin Configuration

QFN PIN LIST

Pin index	Pin count	Name	Type	Purpose
1-12	12	VIN	Analog Input	Amplifier input
25-36	12	VOUT	Analog Output	Required 100k/330nF filter
13,48,PAD	3	VSS	Power	Negative high voltage power supply (-5V to -10V)
14,47	2	VCC	Power	Positive high voltage power supply (5V to 10V)
15	1	VSSA	Analog Input	Offset control pin. Connect to VSS
16	1	EXC	Digital Output	Carrier generator output (frequency = CLK/128)
17-20	4	PHASE_OUT	Digital Output	Phase output
21,24,38,45	4	GND	Ground	System ground
22,37,43	3	VDD	Power	Digital (control) and low voltage amplifier (3.3V)
23	1	VREF	Analog Input	Reference for output amplifier (1.65V)
39	1	MISO	Digital Output	SPI interface: Master in Slave out
40	1	MOSI	Digital Input	SPI interface: Master out Slave In
41	1	SSB	Digital Input	SPI interface: Slave select
42	1	MCLK	Digital Input	SPI interface: Master clock
44	1	SYNC	Digital Input	External demodulator (Sync)
46	1	CLK	Digital Input	Reference clock
Total	49			

ORDERING GUIDE

Model[1]	Operating Temperature	Package Description	MSL Peak Temp[2]
CDI12100[1]	-20°C to 85°C	QFN	Level-3-260C-168 HR

[1] All models are RoHS compliant part.

[2] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

REVISION HISTORY

REV	DATE	DESCRIPTION
A	1/2024	Preliminary release